

Compal Confidential

FH50Q MB Schematics Document

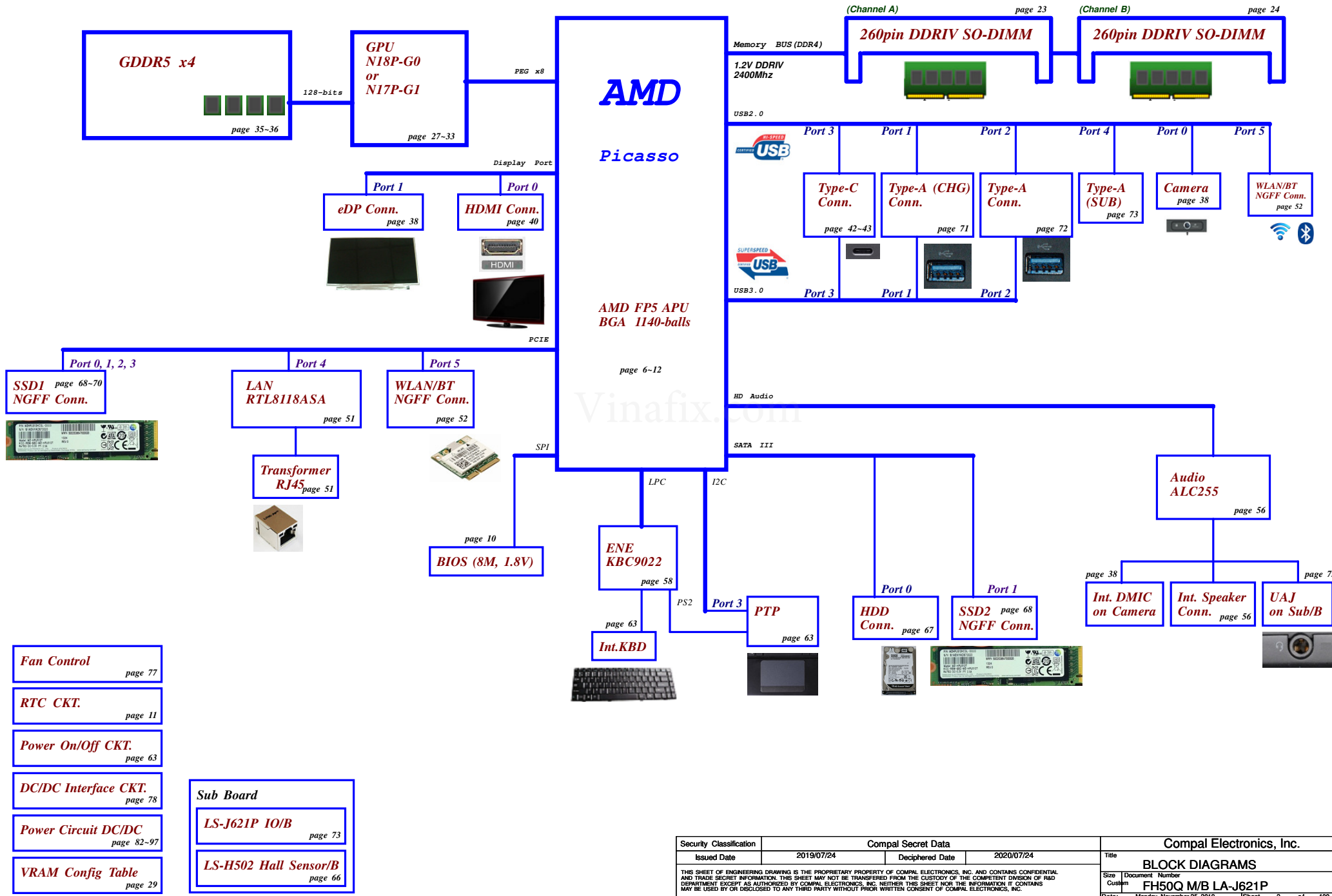
AMD Picasso Platform

nVidia N17P-G1 & N18P-G0

LA-J621P REV:1.0

2019-11-26

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2019/07/24	Deciphered Date	2020/07/24	Title	
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				Size	Document Number
				Custom	FH50Q M/B LA-J621P
				Date:	Monday, November 25, 2019
				Sheet	1 of 100
				Rev	1.0



Power Plane	Description	S0	S3	S5
+19V_VIN	Adapter power supply (19V)	ON	ON	ON
+19VB	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_SOC	Core voltage for APU	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail for APU and DDR	ON	ON	OFF
+1.2V	1.2V power rail for APU and DDR	ON	ON	OFF
+0.6VS	0.6V switched power rail for DDR terminator	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+0.9VALW	0.9V always on power rail	ON	ON	ON
+0.9VS	0.9V switched power rail	ON	OFF	OFF
+RTC_APU	RTC power	ON	ON	ON
+3V_LAN	3.3V LAN IC power	ON	ON	OFF
+TP_VCC	3.3V Touch Pad power	ON	ON	OFF
+FP_VCC	3.3V Finger Print power	ON	ON	OFF
+3VSDGPU	VGA power	ON	OFF	OFF
+1.8VSDGPU_AON	VGA power	ON	OFF	OFF
+1.8VSDGPU_MAIN	VGA power	ON	OFF	OFF
+1.3VSDGPU	VGA power	ON	OFF	OFF
+1.0VSDGPU	VGA power	ON	OFF	OFF
+NVVDD1	VGA power	ON	OFF	OFF

Master	Device	Address[7:1]	Address [7:0]	
			Write	Read
I2C Port 0 (+1.8VS)				
I2C Port 1 (+1.8VS)				
I2C Port 2 (+3VS)				
SBMUS Port 0 (+3VS)	JDIMM1	0101 0000b 50h	1010 0000b A0h	1010 0001b A1h
	JDIMM2	0101 0001b 51h	1010 0010b A2h	1010 0011b A3h
I2C Port 3 (+3VALW)	PTP (Synaptics)	0010 1100b 2Ch	0011 1000b 58h	0011 1001b 59h
	PTP (ELAN)	0001 1111b 15h	0011 1110b 3Eh	0011 1111b 3Fh
SMBus Port 1 (+3VALW)				

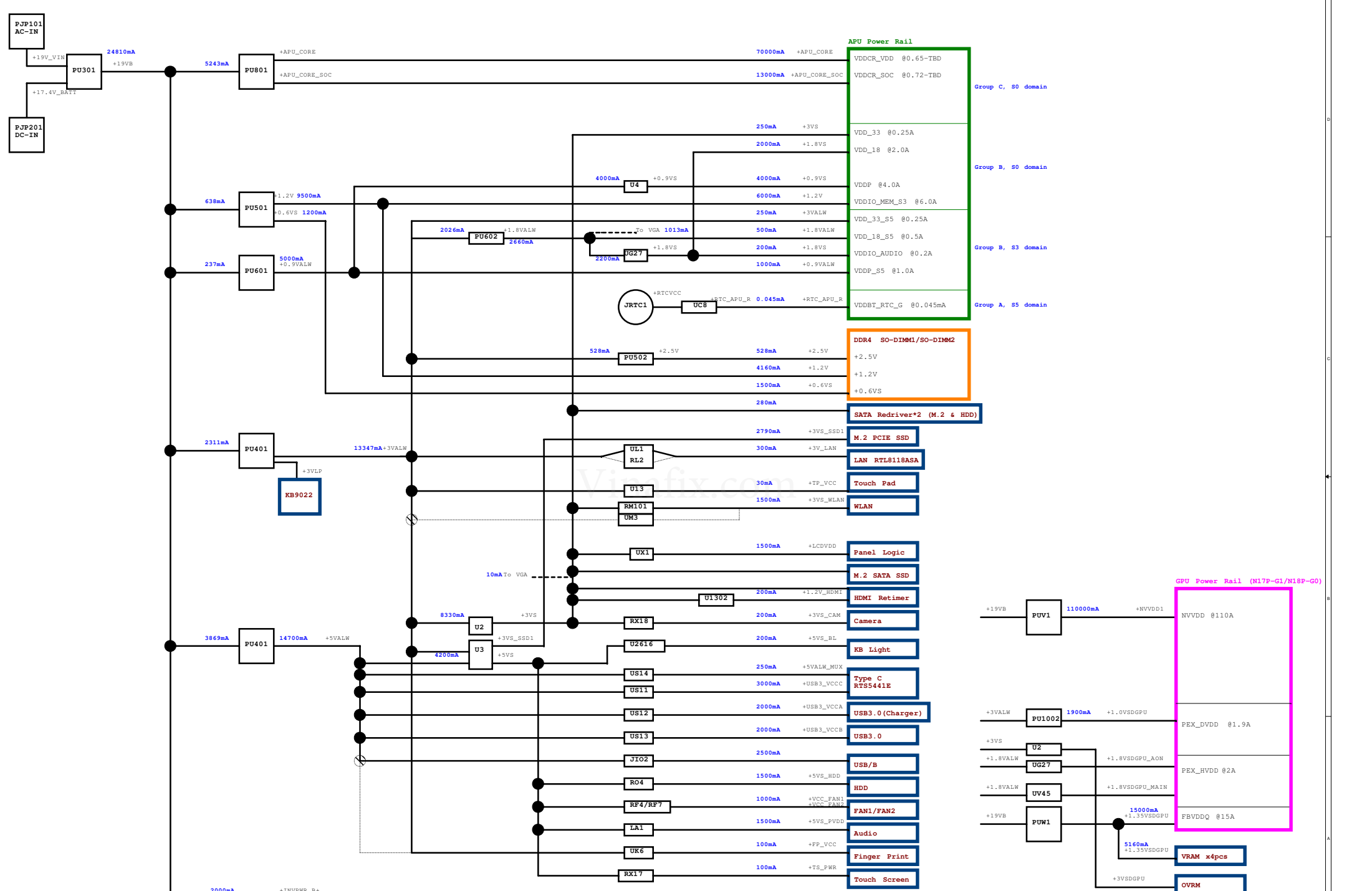
Board ID	PCB Revision
0	EVT
1	PVT

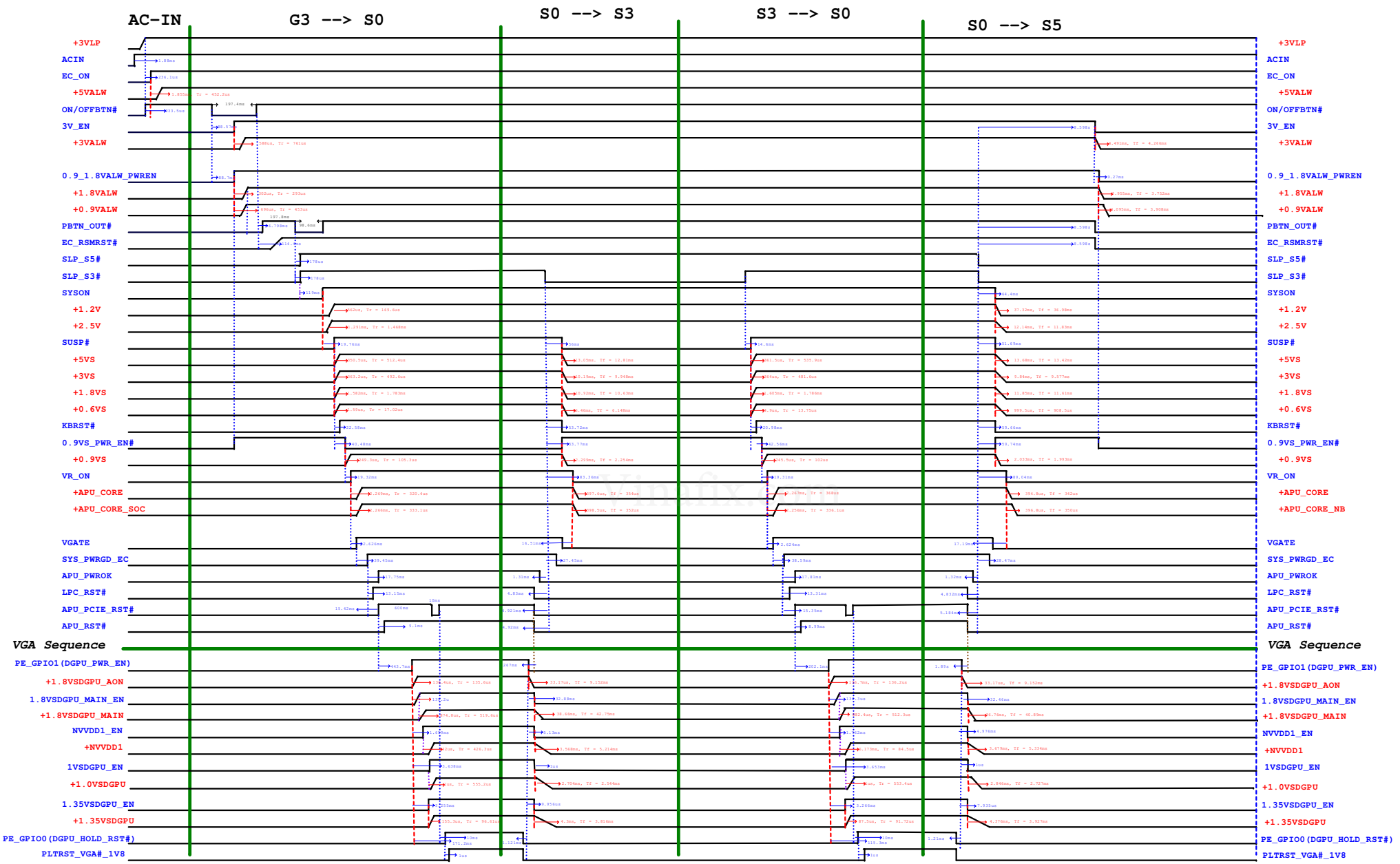
BOM Structure	BTO Item
@	Unpop
EMC@/@EMC@	EMI/ESD Pop/Unpop
45@	HDMI Royalty
CONN@	Mechanical Connector
JP@	Jump
RS@	R-Short
TP@	Test Point
LDO@/SWR@	RTL8118ASA Switching-Mode only
R5/R7APUQC@	APU PN Refer p.6
R5/R7APU@	APU PN Refer p.6
TMS@	Thermal Sensor
TMSIEC@	Thermal Sensor for IEC safety
EVT@/PVT@/MP@	Test BOM for EVT/PVT/MP
KBLED@/LED14P@	Keyboard back light / RGB back light
N17P@	N17P-G1
N18P@	N18P-G0
DIS@	VGA Circuits
VRAM4G@	GDDR5*4
GC6@/NGC6@	nVidia DGPU GC6 2.0
ON_X76@	OVRM-ON
uPI_X76@	OVRM~uPI*

SMBus Port 1 (+3VALW)	Smart Battery	0000 1011b 0Bh	0001 0110b 16h	0001 0111b 17h
	Charger IC (BQ24735)	0000 1001b 09h	0001 0010b 12h	0001 0011b 13h
SMBus Port 2 (+3VS)	APU Temp. (TS1)	0100 1100b 4Ch	1001 1000b 98h	1001 1001b 99h
	GPU Temp.	1001 1110b 9Eh		
	Thermal Sensor G781-1		1001 1010b 9Ah	1001 1011b 9Bh
	Thermal Sensor IEC 62368-1		1001 0000b 90h	1001 0001b 91h
SMBus Port 3 (+3VALW)	LED driver		1100 0000b C0h	1100 0001b C1h

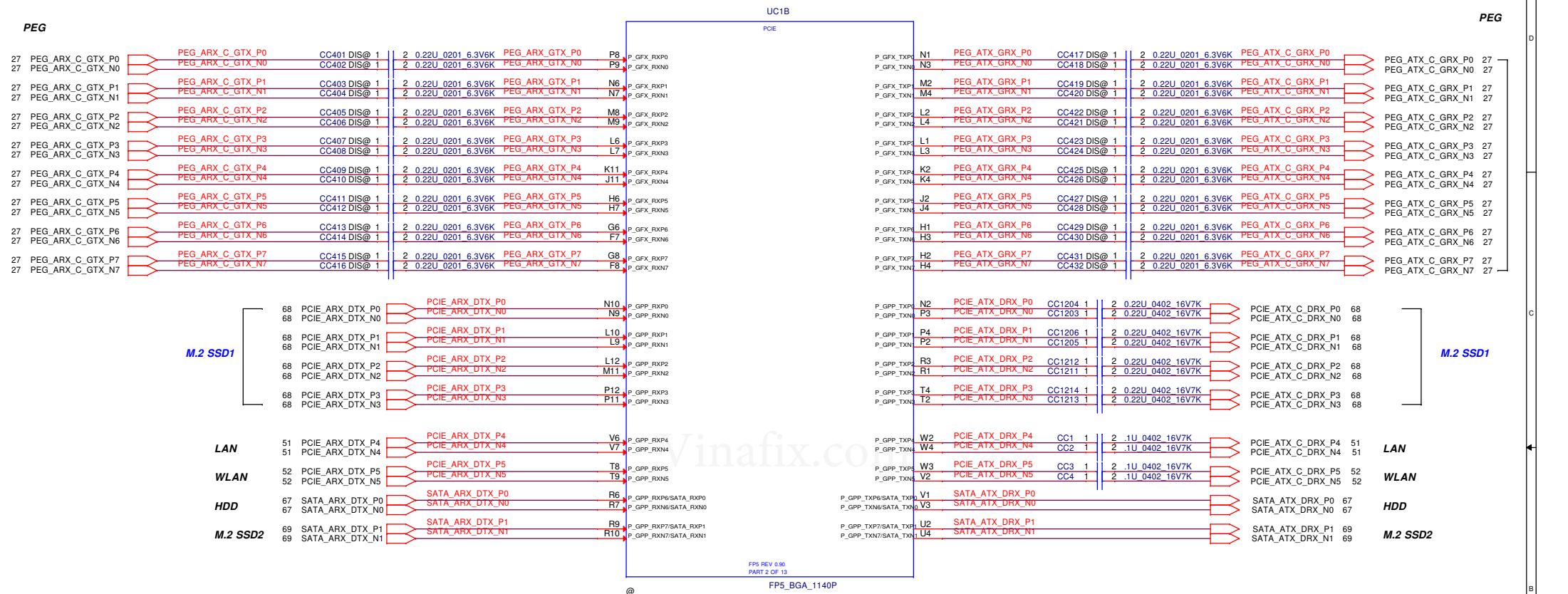
Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb	V min	V typ	V max	EC AD
0	0		0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V		0xE7 - 0xFF

Group	Parameter	Value
G~A	+RTC_BATT	
	EC_ON	
	+5VALW	
	3V_EN	
G~B	+3VALW	
	0_9_1.8VALW_PWREN	
	+1.8VALW/+0.9VALW	
G~C	SYSON	
	+1.2V/+2.5V	
	SUSP#	
	+5VS/+3VS/+1.8VS/+0.6VS	
	0.9VS_PWR_EN#	
	+0.9VS	
G~D	VR_ON	
	+APU_CORE	
	+APU_CORE_SOC	









Main Func = CPU



APU PN Table

APU Platform	Customer PN	Customer PN	Customer PN	Customer PN	Compal PN	Compal PN
Picasso	UC1 R5APUQC@  S IC RYZEN5 YM3500C4T4MFG 2.1G BGA APU SA0000CCR20	UC1 R7APUQC@  S IC RYZEN7 YM3700C4T4MFG 2.3G BGA APU SA0000C7640	UC1 R5APU@  S IC RYZEN5 YM3500C4T4MFG 2.1G APU ABO! SA0000CCR60	UC1 R7APU@  S IC RYZEN7 YM3700C4T4MFG 2.3G APU ABO! SA0000C7680		

PCB Number

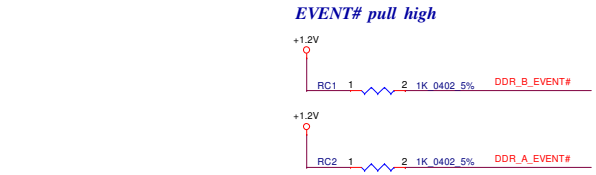
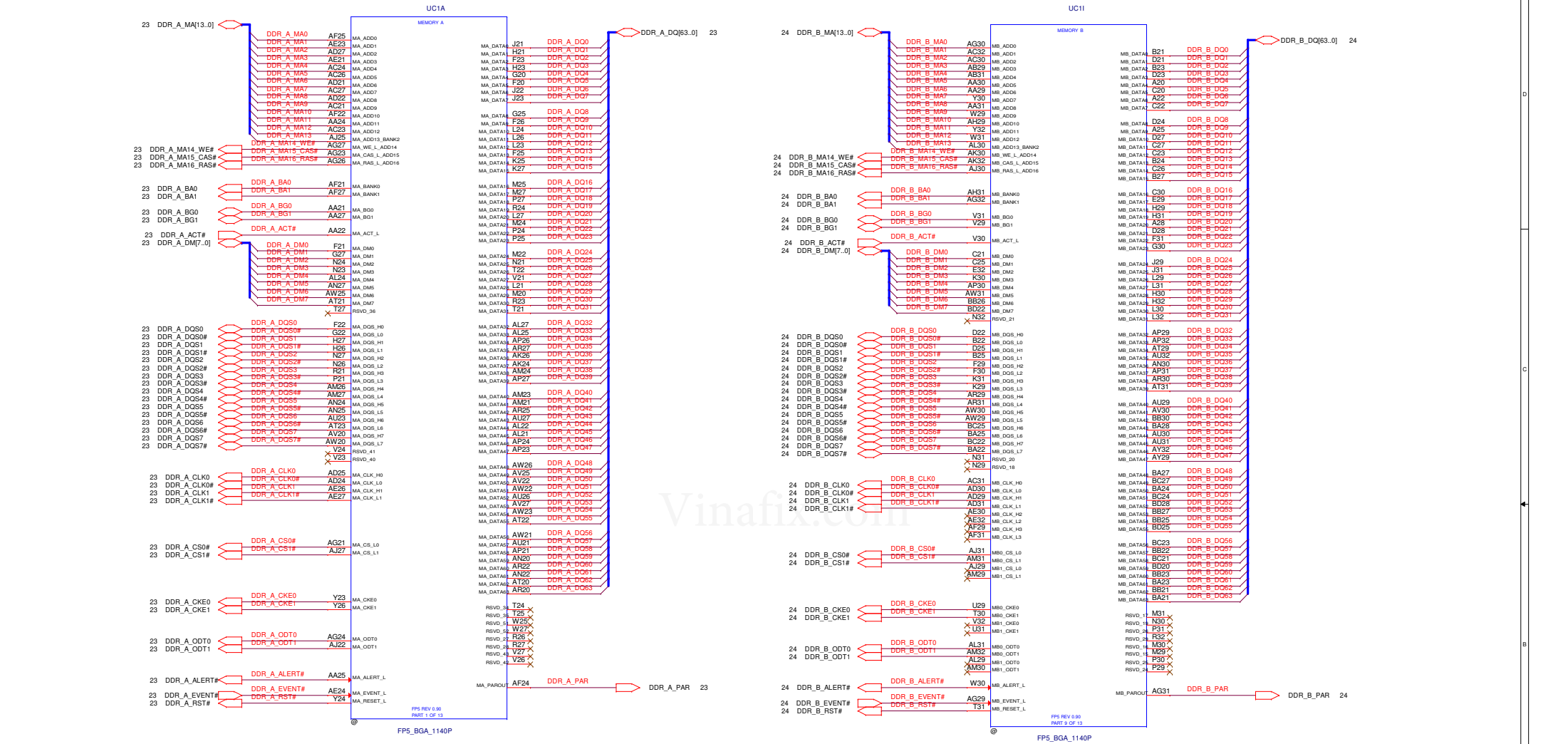
ZZZ EVT@
PCB 2WM LA-J621P REV0 MB 2
DA8001LZ000

ZZZ1 PVT@
PCB FH50Q LA-J621P LS-J621P/H502P
DAZ2WM00100

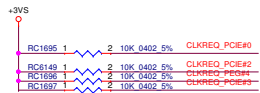
ZZZ2 MP@
PCB FH50Q LA-J621P LS-J621P/H502P
DAZ2WM00100

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				Date:	Monday, November 25, 2019
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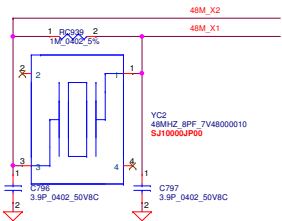
Main Func = CPU



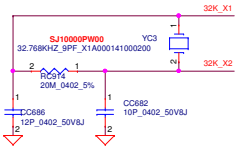
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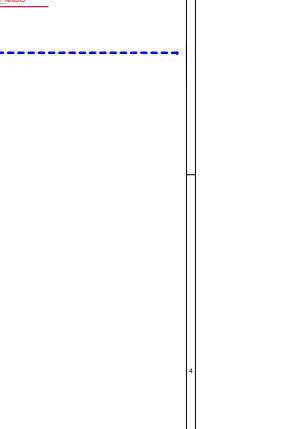
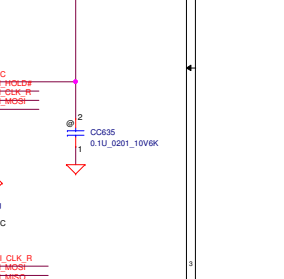
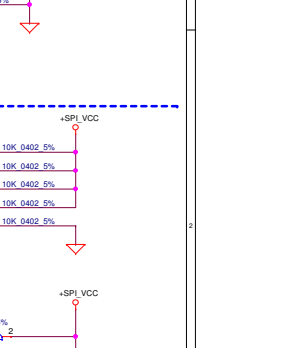
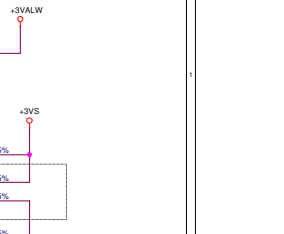
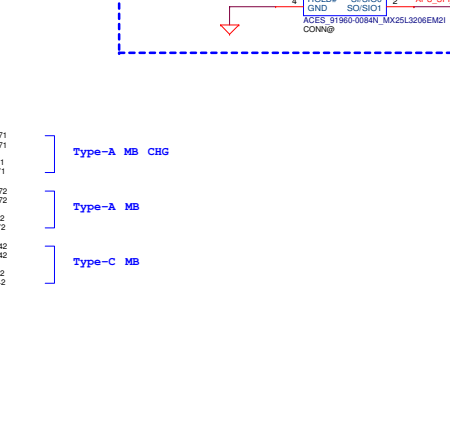
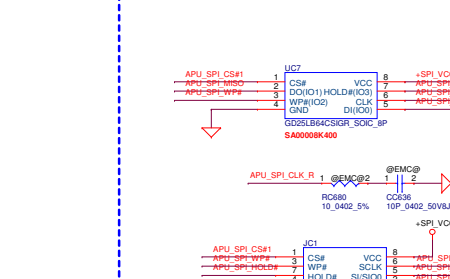
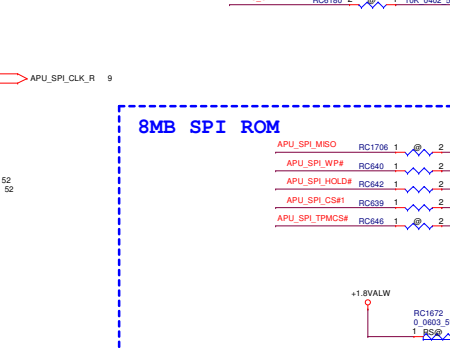
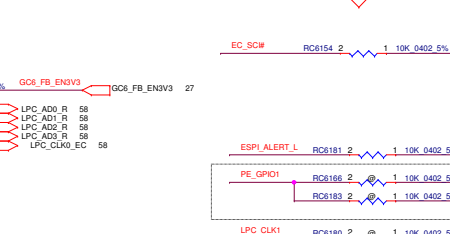
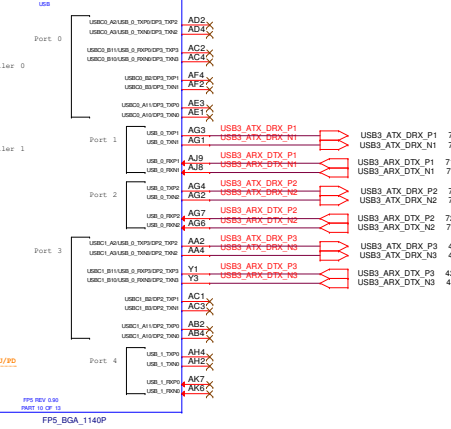
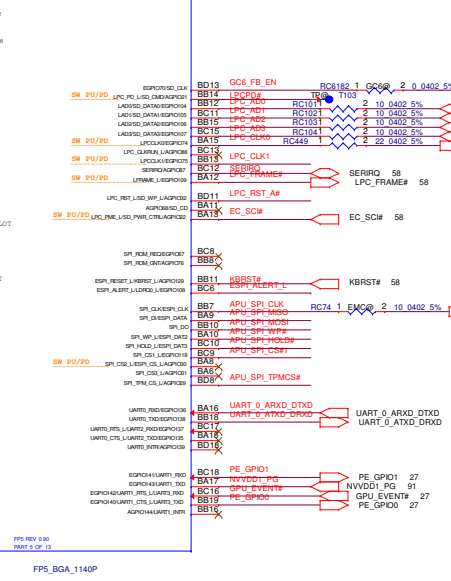
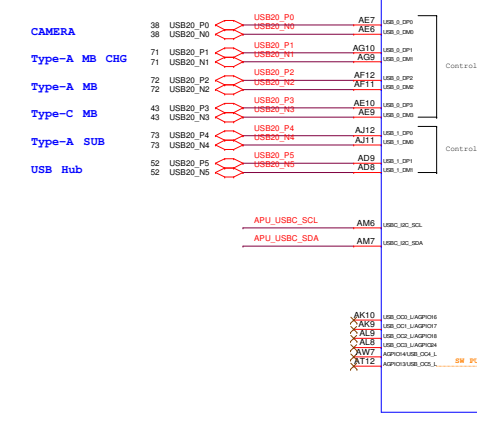
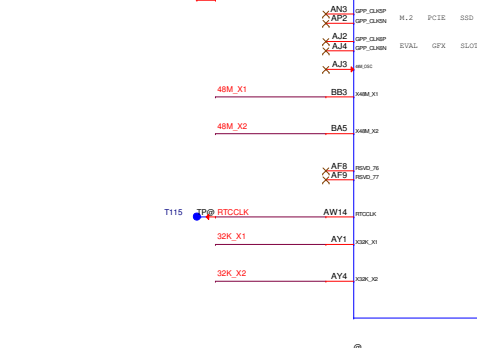
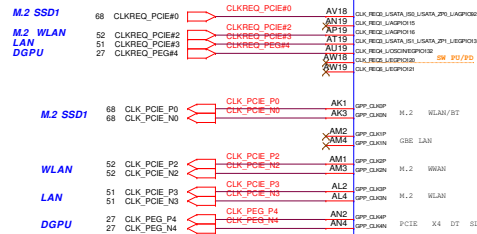
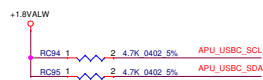
48MHz CRYSTAL



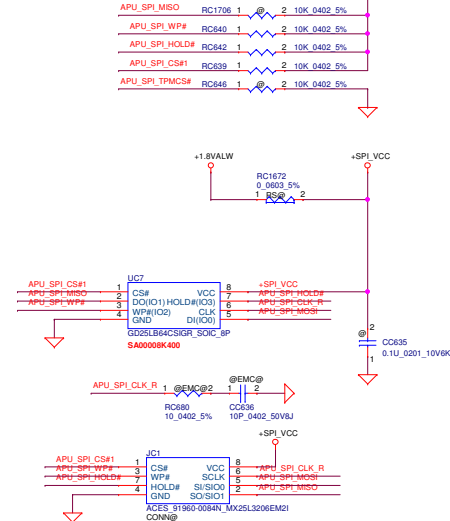
32.768KHz CRYSTAL



USB Function

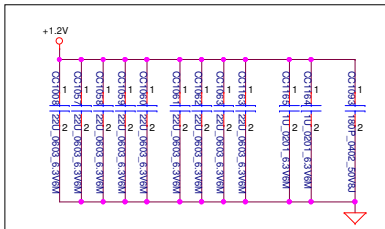


8MB SPI ROM

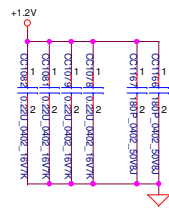


Main Func = CPU

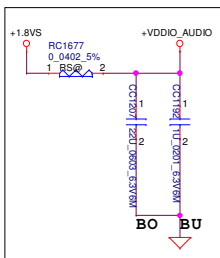
```
+APU_CORE_SOC Cap
place at Power Side
```



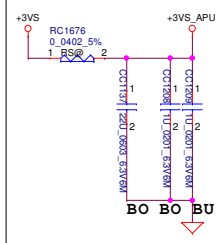
All BU(on bottom side under SOC)



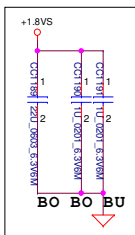
ACROSS VDDIO AND VSS SPLIT



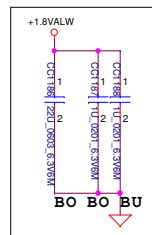
SCL/MBDG:
1 *22uF (B
1*1uF (BU)



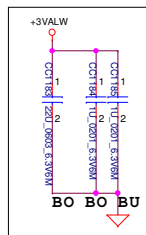
SCL/MBDG:
1 *22uF (BO)
2*1uF (BO+BU)



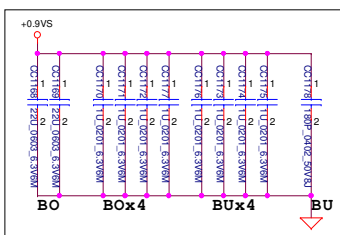
+1.8VALW



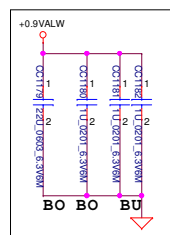
+3VALW



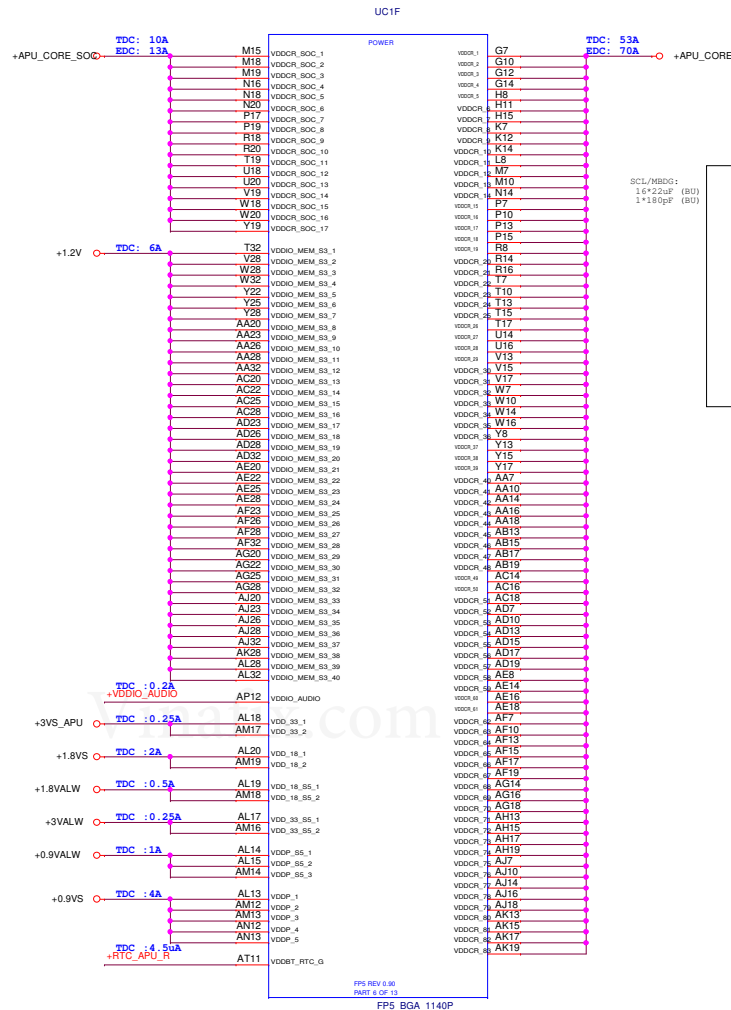
SCL/MBDG:
1 *22uF (BO)
2*1uF (BO+BU)



SCL/MBDG:
2 *22uF (BO)
8*1uF (BOx4+BUx4)
1*180pF (BU)



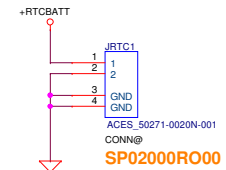
SCL/MBDG:
1 *22uF (BO)
3*1uF (BOx1+BUx2)



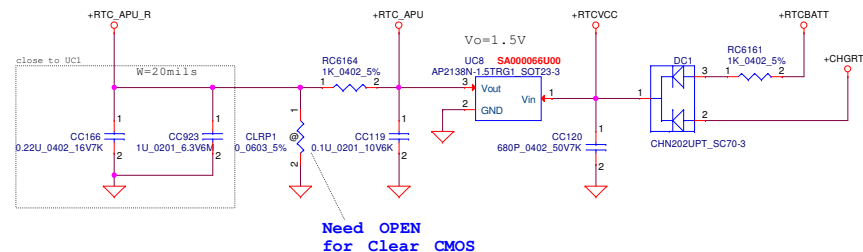
SCL/MBDG:
16*22uF (BU
1*180pF (BU

```
+APU_CORE Cap place at Power Side
```

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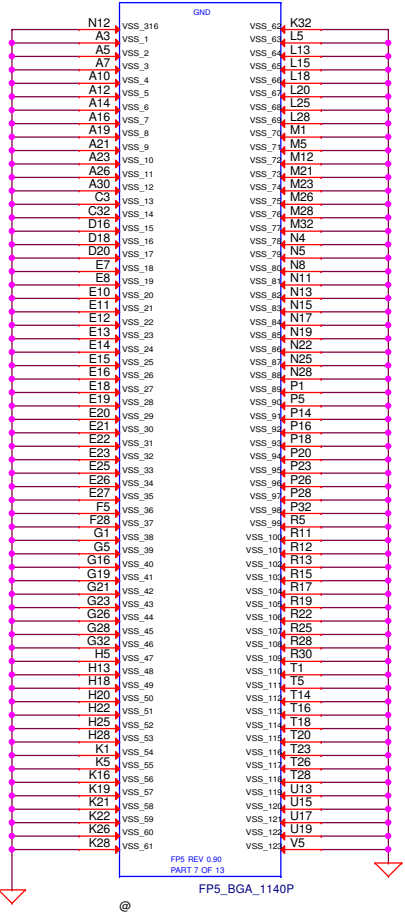
RTC OF APU



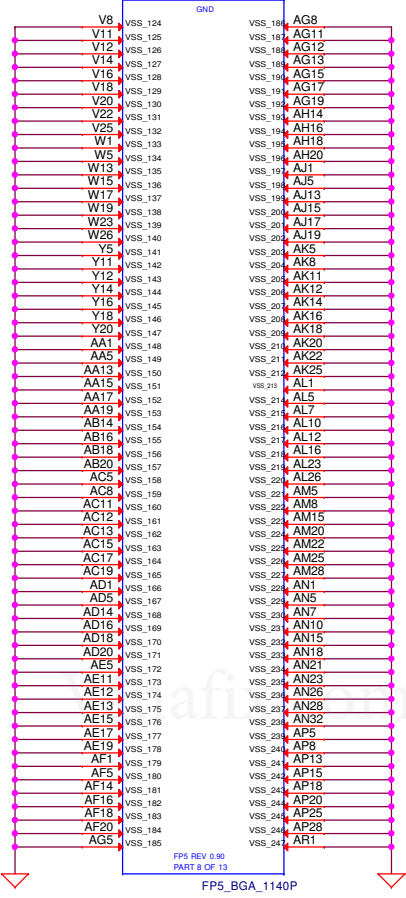
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Main Func = CPU

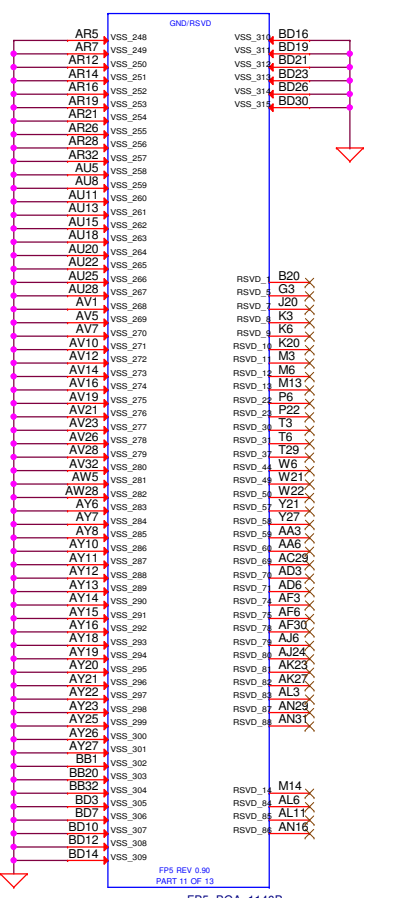
UC1G



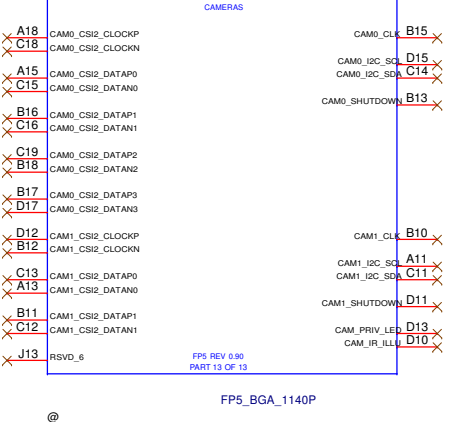
UC1H



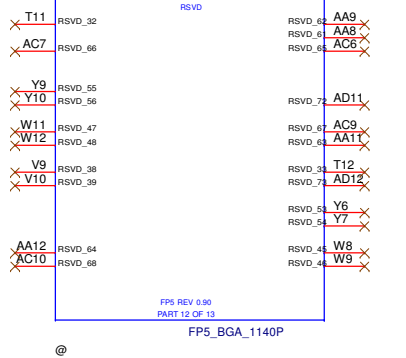
UC1K



UC1M



UC1L



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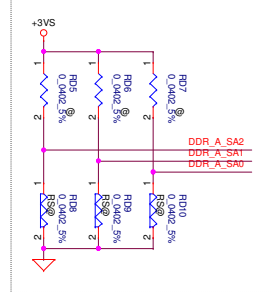
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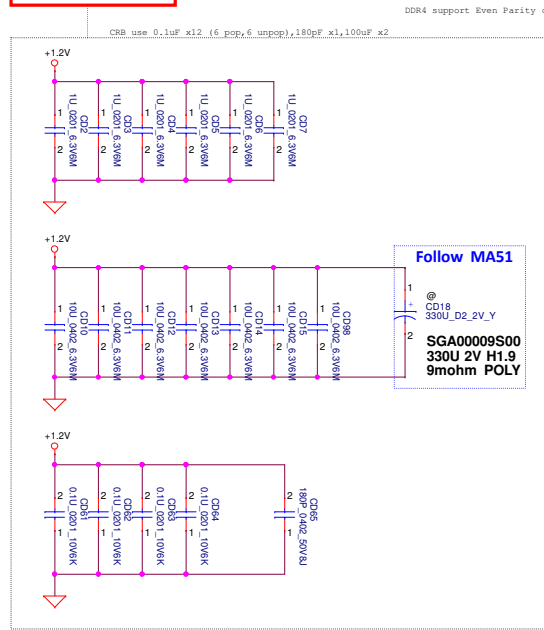
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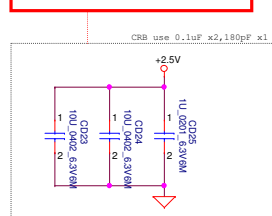


Layout Note:
Place near JDIMM1

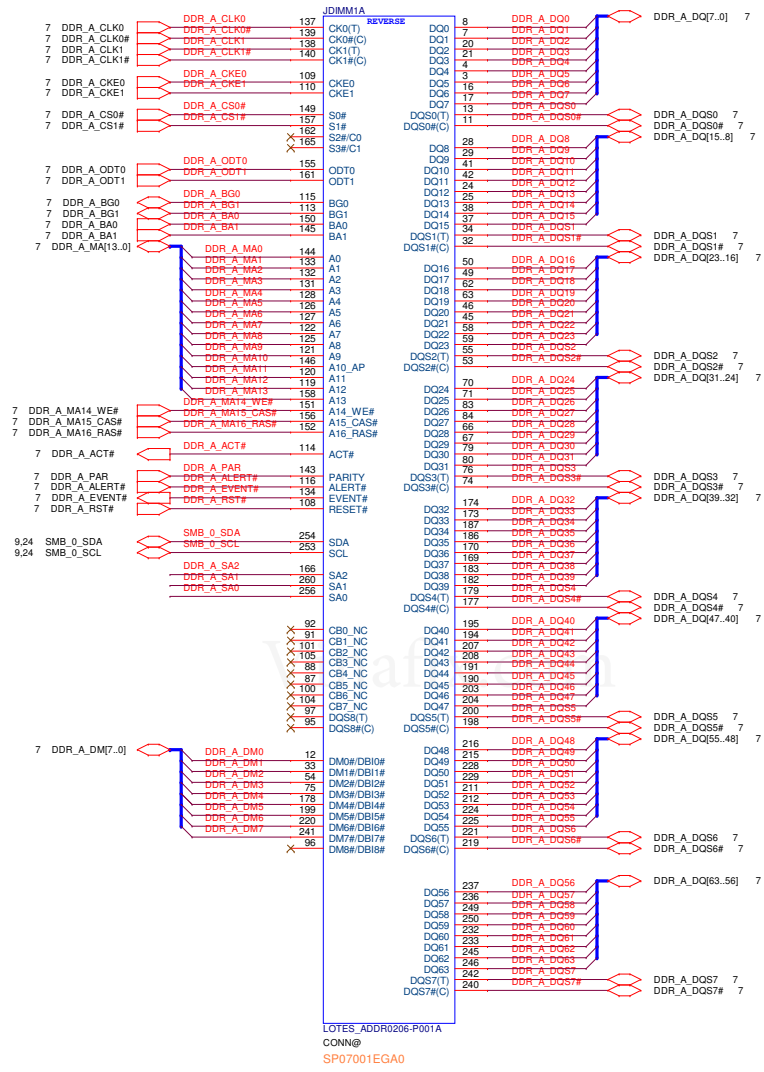
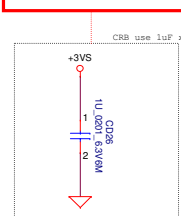
Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket



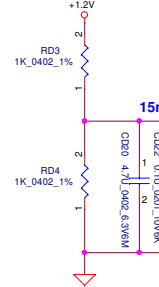
Layout Note:
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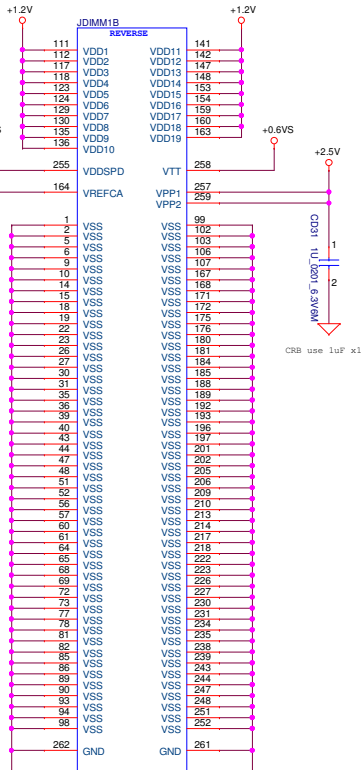
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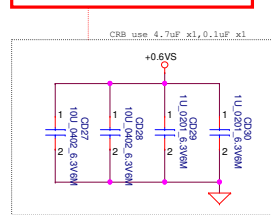
Follow CRB design



Place near to SO-DIMM connector.



Layout Note:
Place near JDIMM1.258



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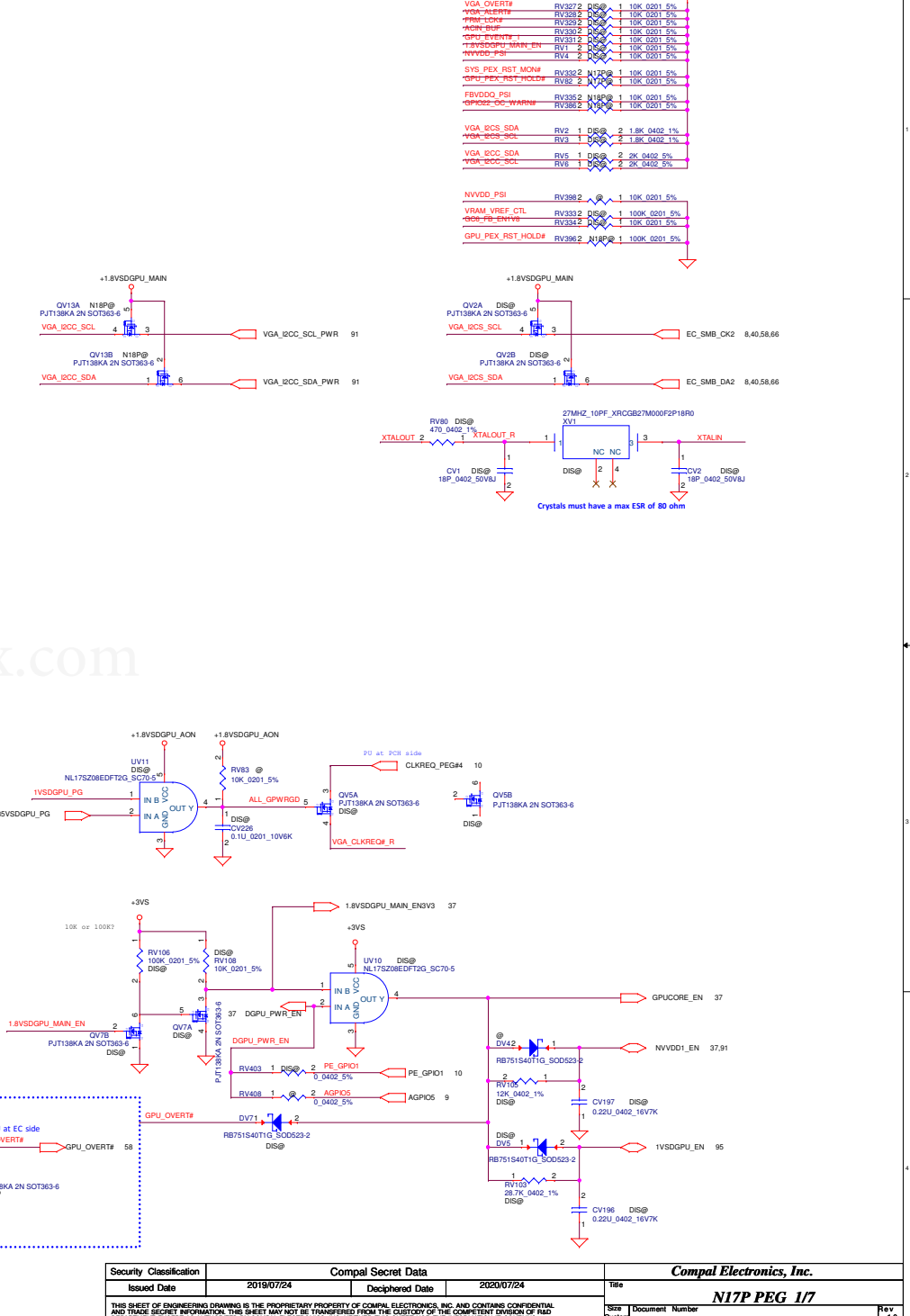
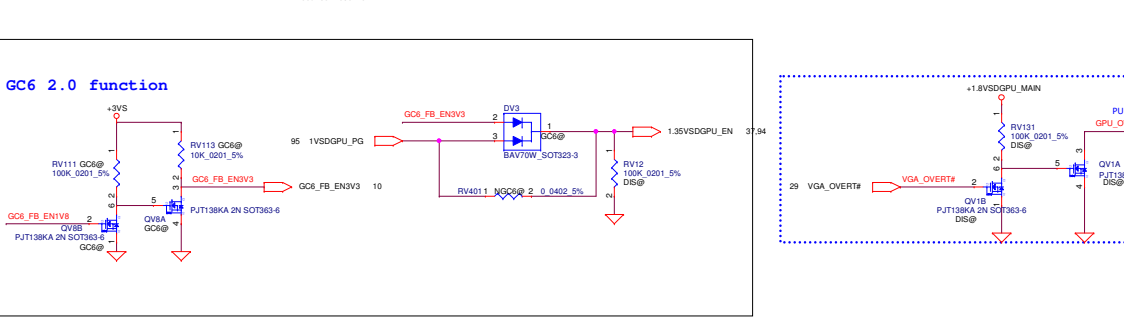
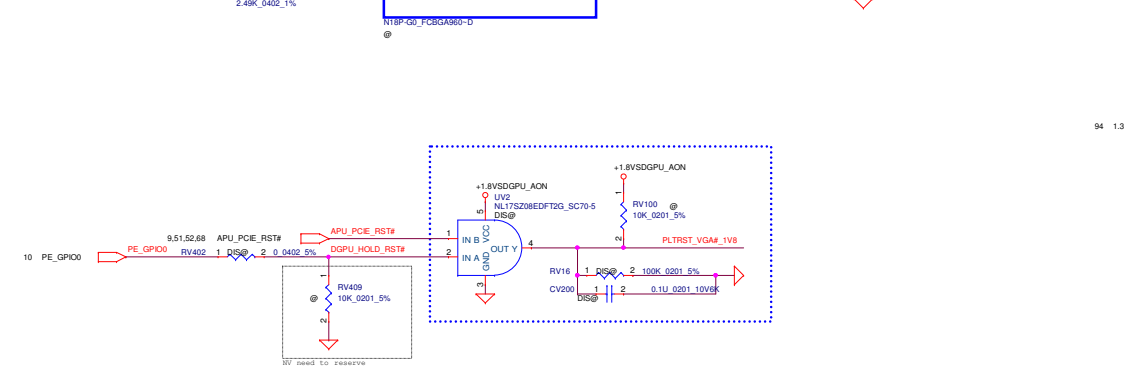
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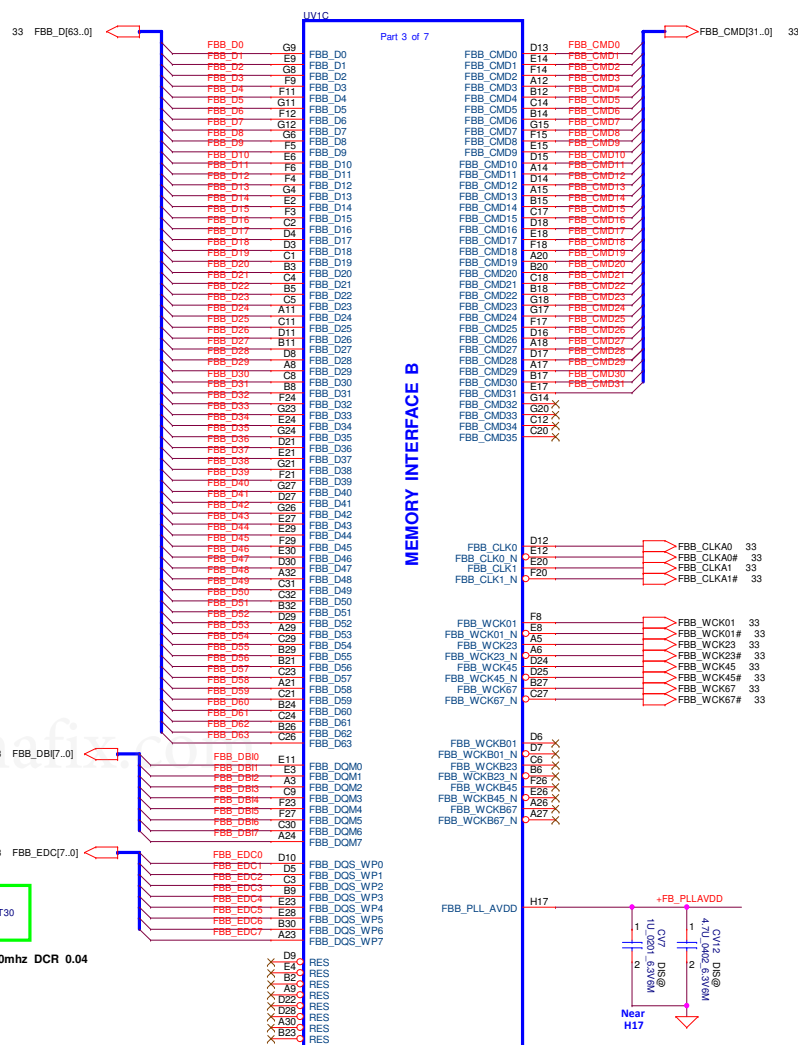
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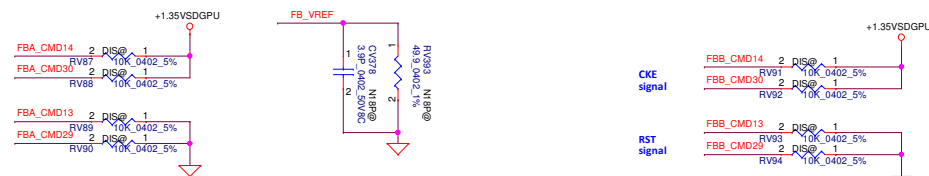
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	DATA Bus	
Address	0...31	32...63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RF
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#





CO K14 CDDRE Recommended Memo

Allowed							
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Allowed			
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Notes:

100

Strap Pins ^{see Note}DA-08920-001_v04

Strap Pin	N17/GB4C-128	N18/GB4D-128
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1. The ROM_SO pin should be pulled low using a 10k-ohm resistor for N18/GB4D-128 GPUs

N18P-G0

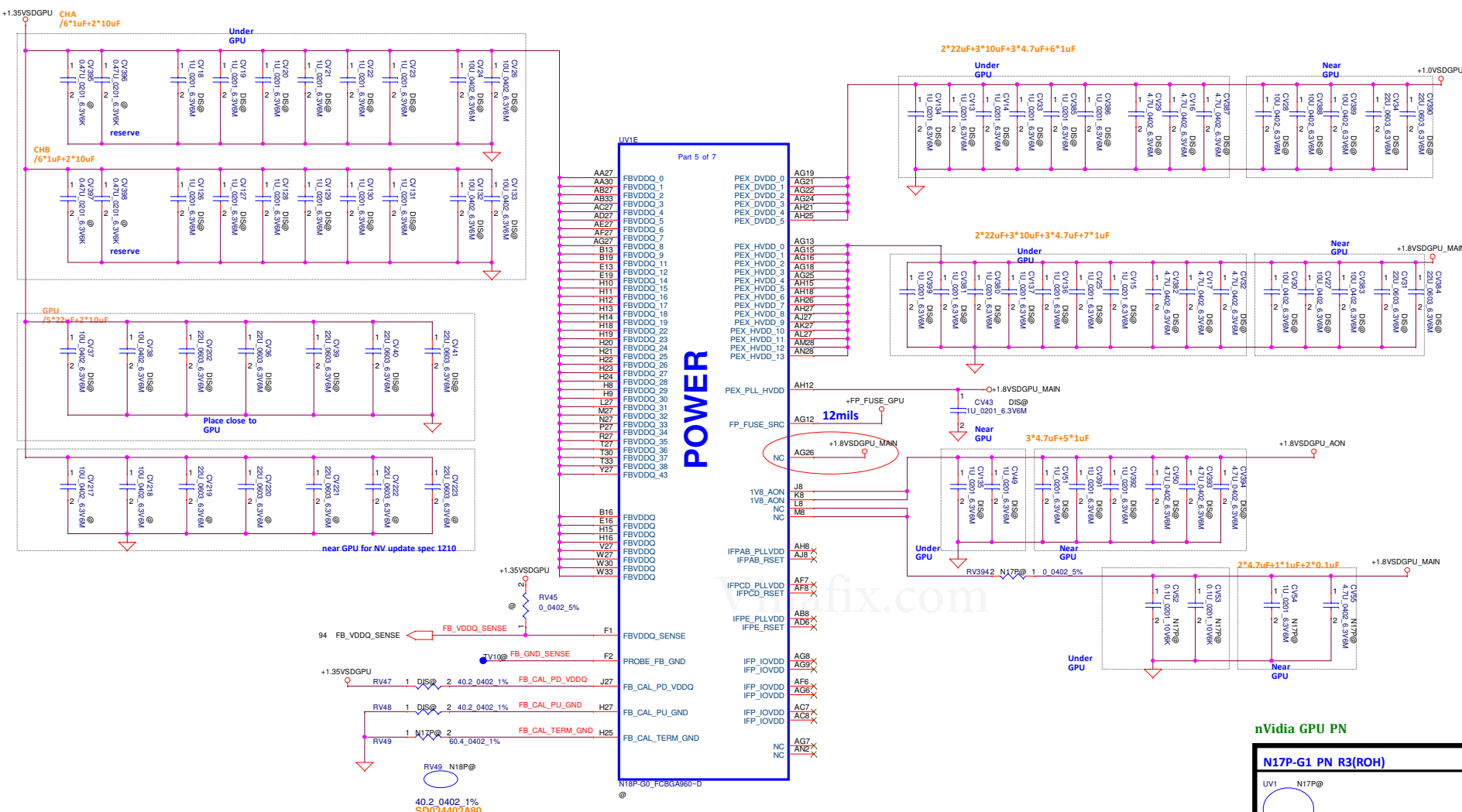
2017	2016	see Note 1	
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N17P-G1

Row	Strap Pins <small>see Note</small>	Resulting SORx_EXPOSED Enablements
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Security Classification	
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Note 1	Functions Selected by This Streaming
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For nVidia N17P-G1 VRAM Device ID: 1C8C/CC

Strap/Vendor/Size	Memory PN R3(ABO!)	STRAP[2:0]
(8Gb) 0x05 HYNIX 256M x32	UV4 X76_H4G@ UV5 X76_H4G@ UV6 X76_H4G@ UV7 X76_H4G@ S IC D5 256M32 H5GC8H24AJR-R2C BGA ABO! SA0000C1700	RV26 X76_H4G@ 100K_0402_5% SD028100380 RV35 X76_H4G@ 100K_0402_5% SD028100380 RV28 X76_H4G@ 100K_0201_5% SD043100380
(8Gb) 0x03 Samsung 256M x32	UV4 X76_S4G@ UV5 X76_S4G@ UV6 X76_S4G@ UV7 X76_S4G@ S IC D5 256M32 K4G80325FC-HC25 FBGA ABO! SA00009TA40	RV26 X76_S4G@ 100K_0402_5% SD028100380 RV27 X76_S4G@ 100K_0402_5% SD028100380 RV36 X76_S4G@ 100K_0201_5% SD043100380

For nVidia N18P-G0 VRAM Device ID: 1F91/D1

Strap/Vendor/Size	Memory PN R3(ABO!)	STRAP[2:0]
(8Gb) 0x02 HYNIX 256M x32	UV4 X76_N18H4G@ UV5 X76_N18H4G@ UV6 X76_N18H4G@ UV7 X76_N18H4G@ S IC D5 256M32 H5GC8H24AJR-R2C BGA ABO! SA0000C1700	RV34 X76_N18H4G@ 100K_0402_5% SD028100380 RV27 X76_N18H4G@ 100K_0402_5% SD028100380 RV36 X76_N18H4G@ 100K_0201_5% SD043100380
(8Gb) 0x04 Samsung 256M x32	UV4 X76_N18S4G@ UV5 X76_N18S4G@ UV6 X76_N18S4G@ UV7 X76_N18S4G@ S IC D5 256M32 K4G80325FC-HC25 FBGA ABO! SA00009TA40	RV34 X76_N18S4G@ 100K_0402_5% SD028100380 RV35 X76_N18S4G@ 100K_0402_5% SD028100380 RV28 X76_N18S4G@ 100K_0201_5% SD043100380

nVidia GPU PN

N17P-G1 PN R3(ROH)

UV1 N17P@

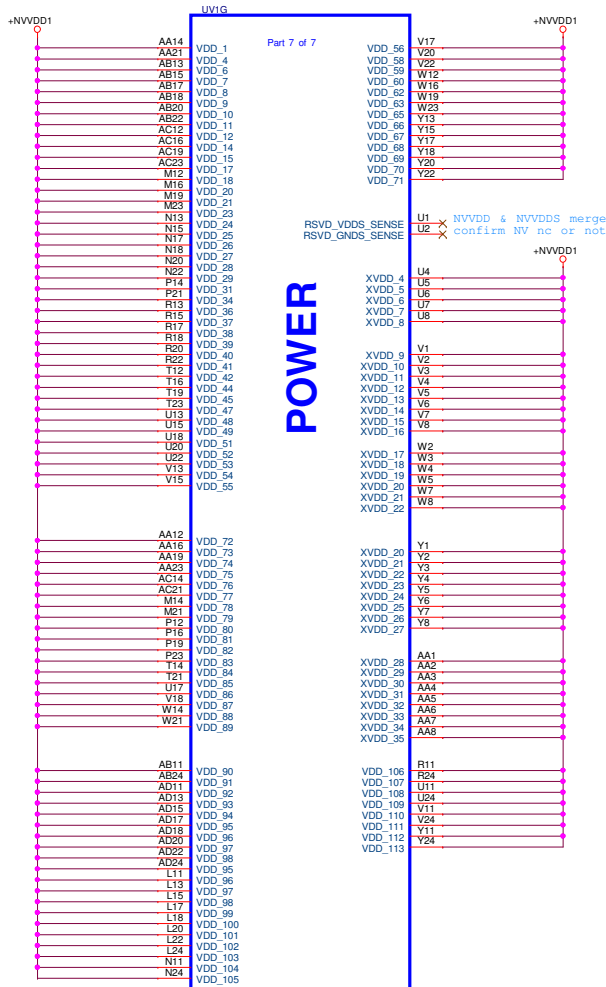
S IC N17P-G1-A1 FCBGA 908P GPU
SA0000A0660

N18P-G0 PN R3(ROH)

UV1 N18P@

S IC N18P-G0-MP-A1 FCBGA 960P GPU
SA0000CZ30

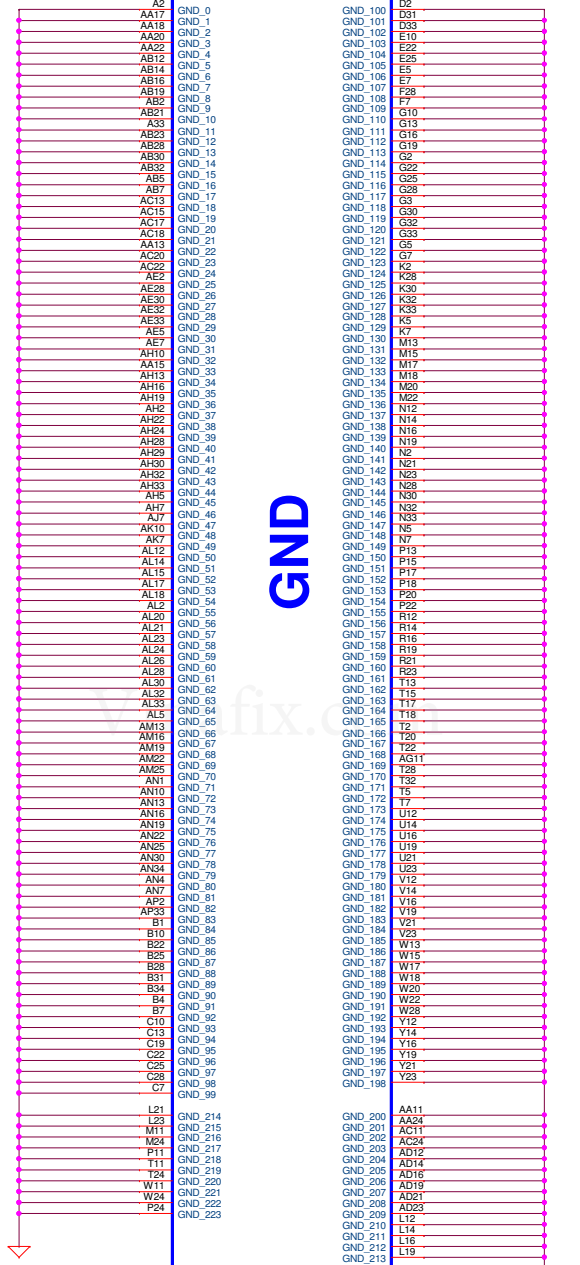
N17P VDD5
1uF*5/4.7uF*5 (under GPU)
330uF*1/22uF*3/10uF*2/4.7uF*2



N18P-G0_FCBGA960-D
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UWIF

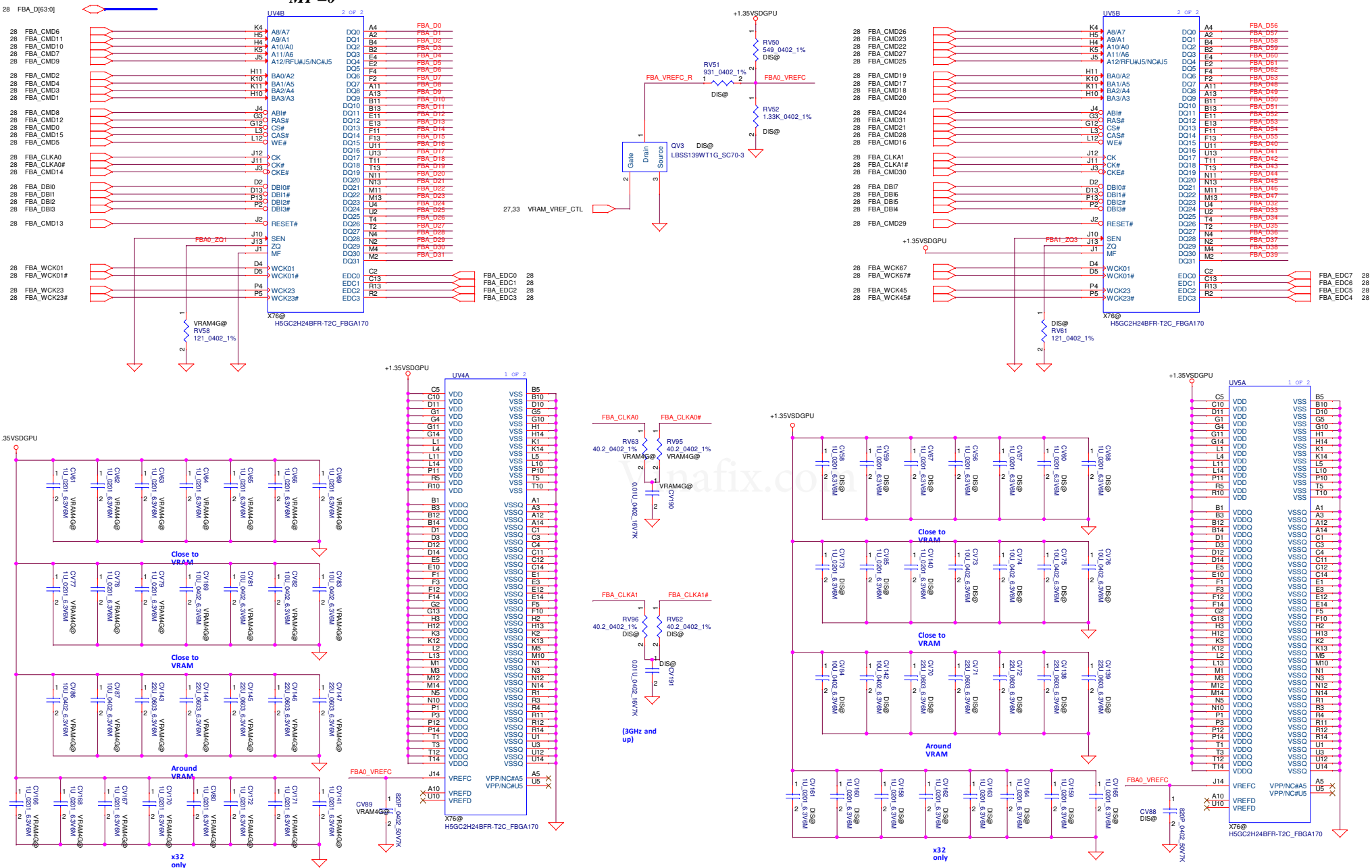
Part 6 of 7



N18P-G0_FCBGA960-D
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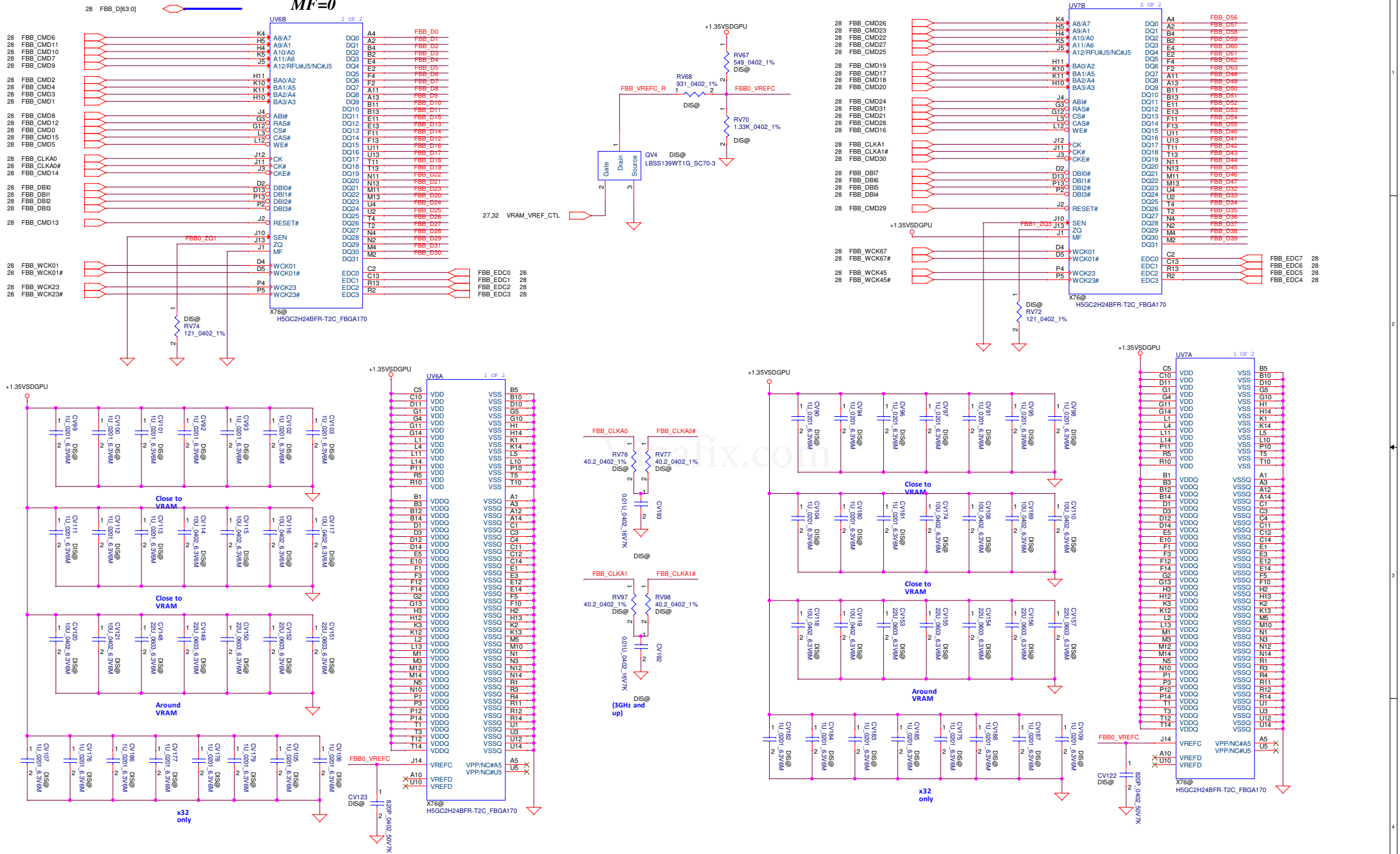
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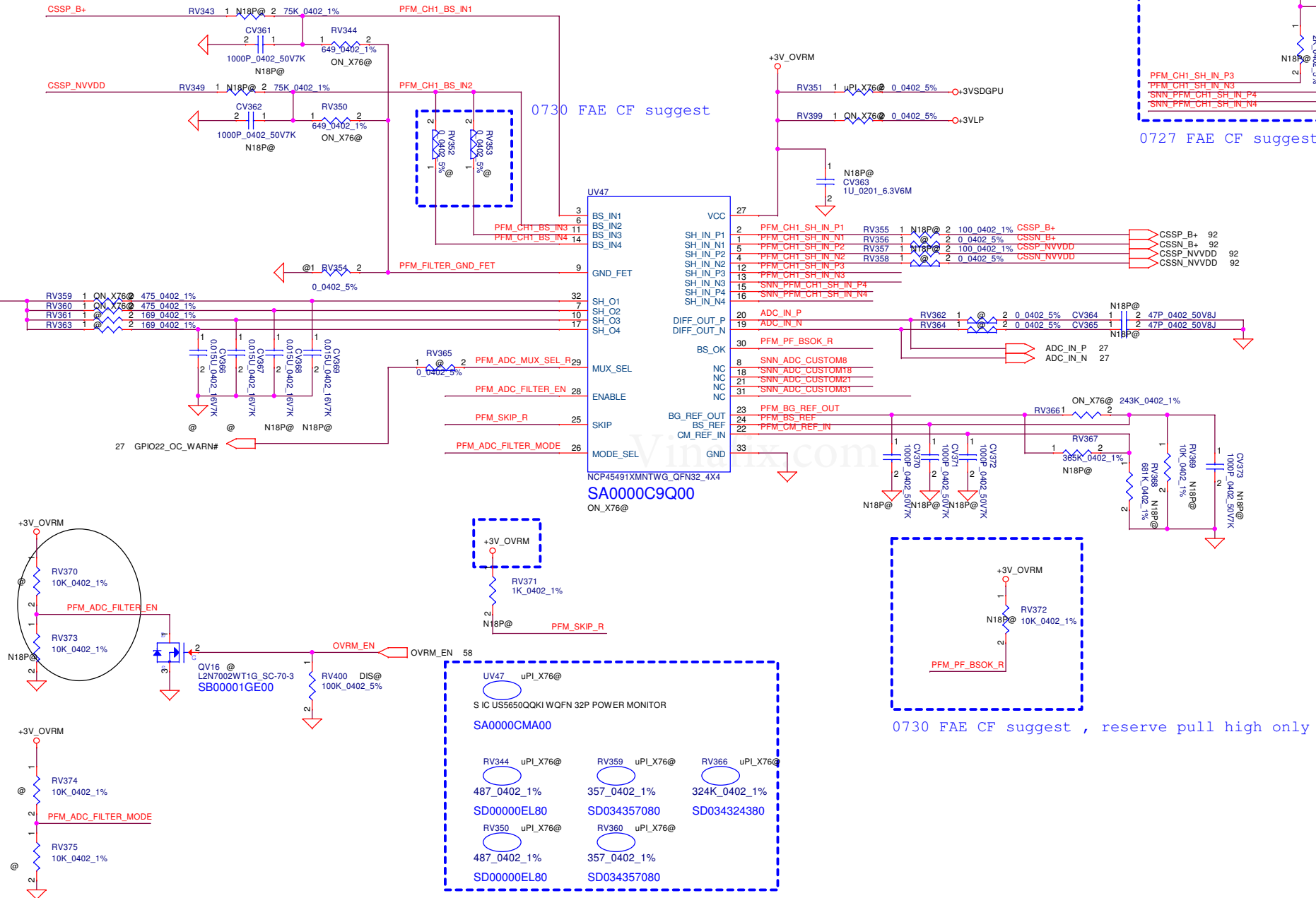
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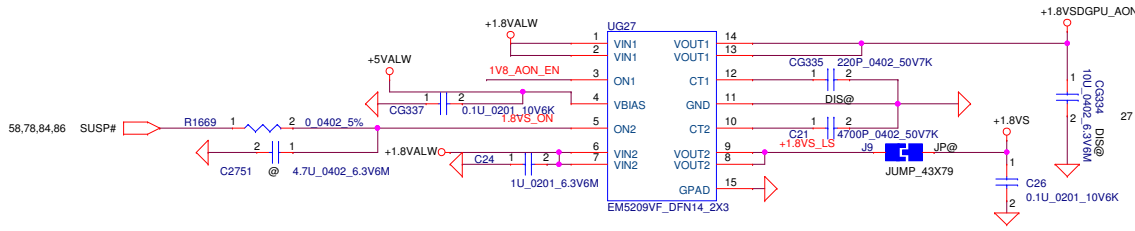
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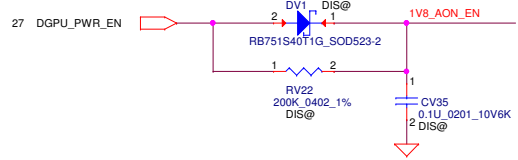


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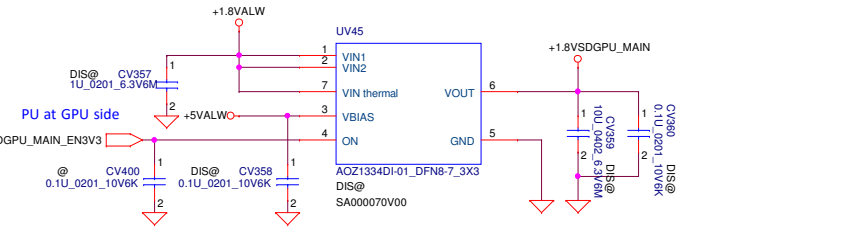
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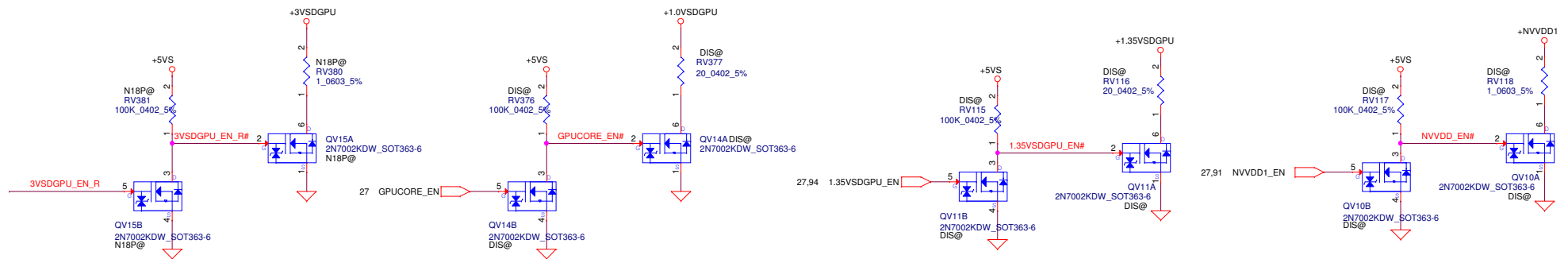
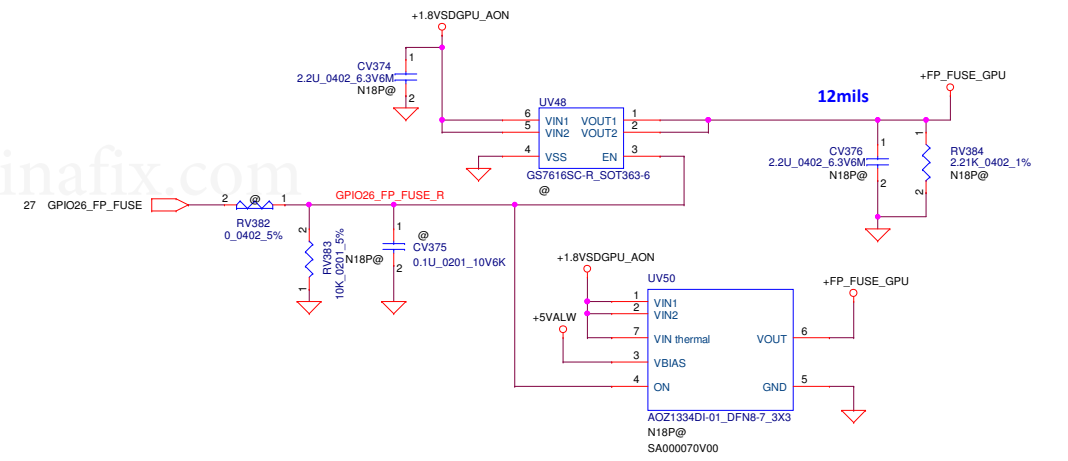
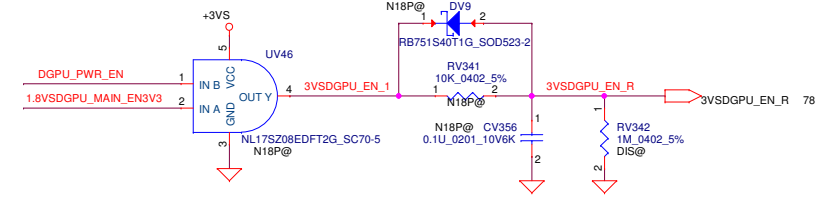
For Power down sequence



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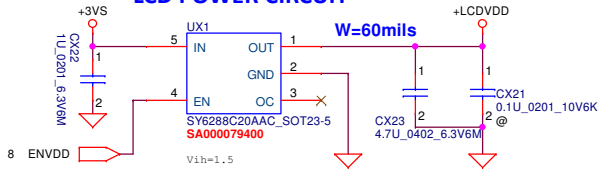


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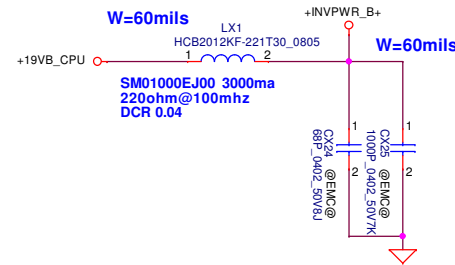
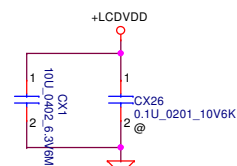


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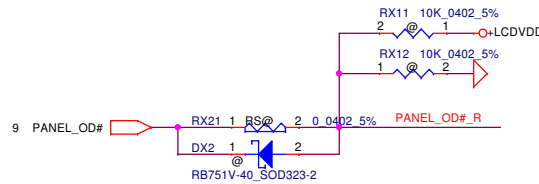
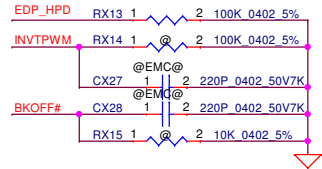
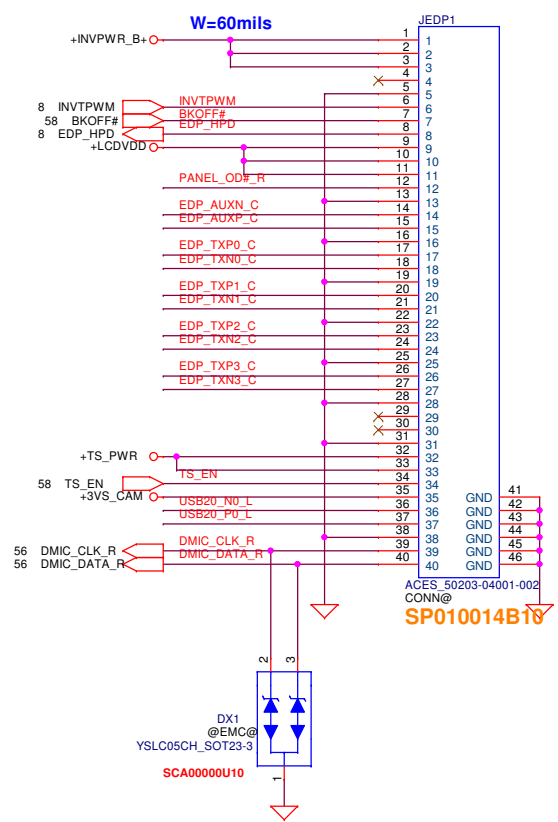
LCD POWER CIRCUIT



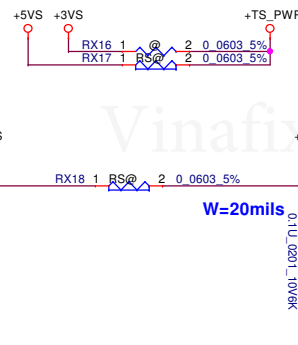
Place closed to JEDP1



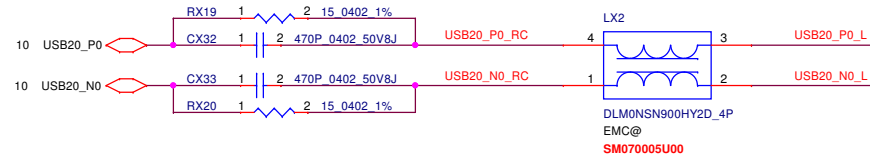
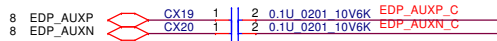
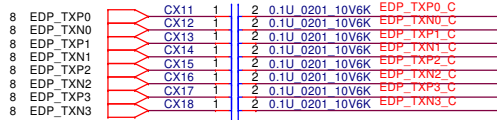
LED PANEL Conn.



Touch Screen



Place closed to JEDP1

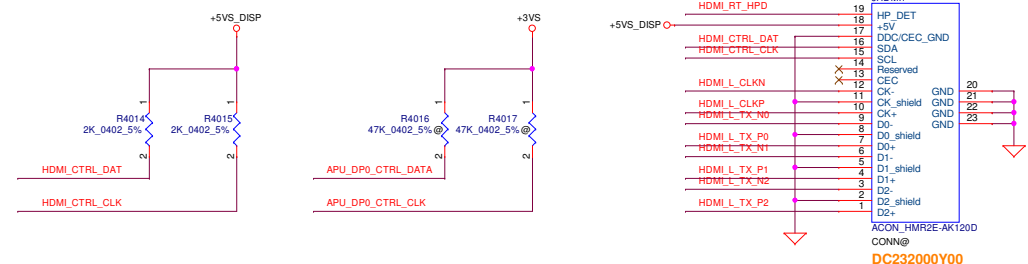
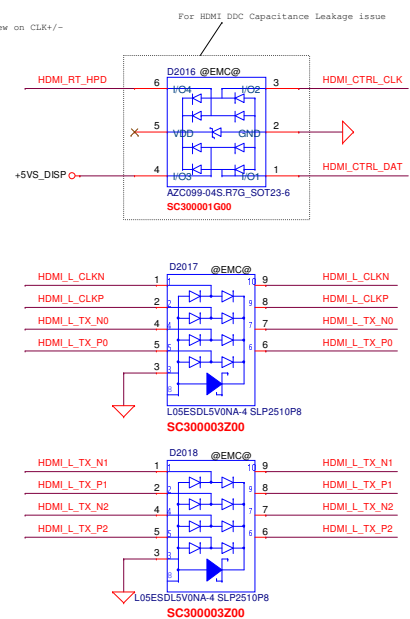


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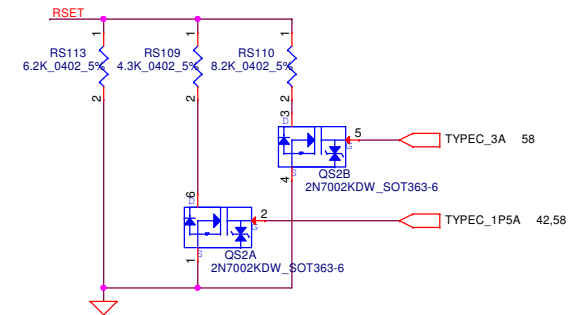
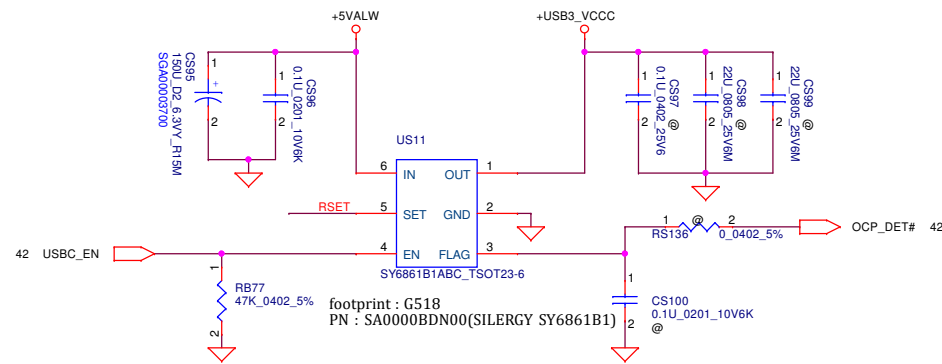


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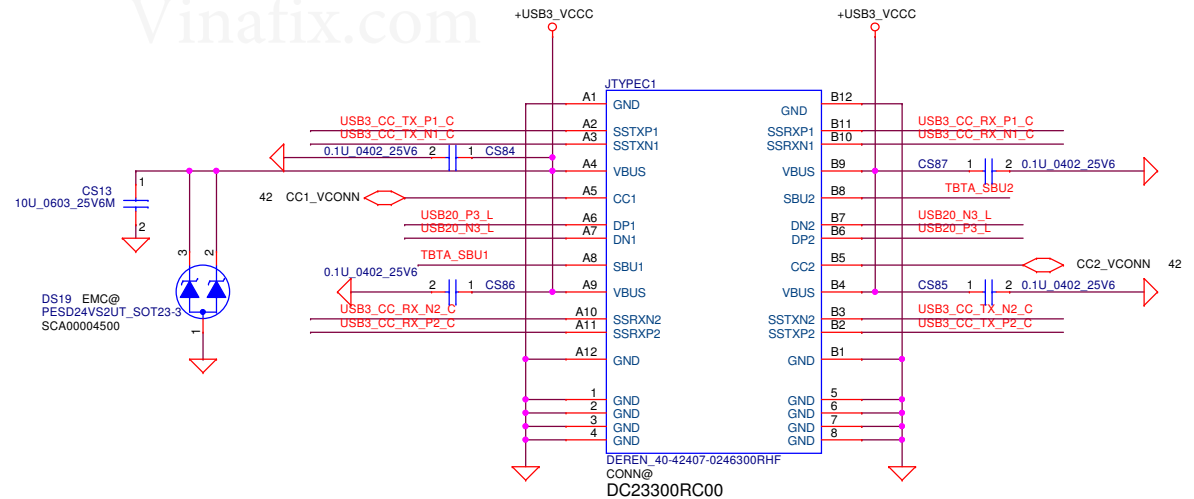
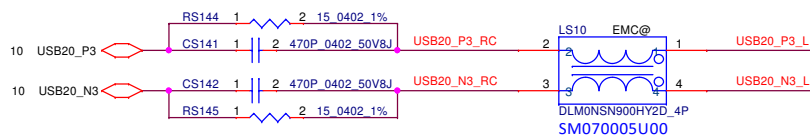
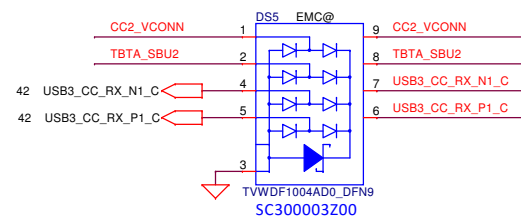
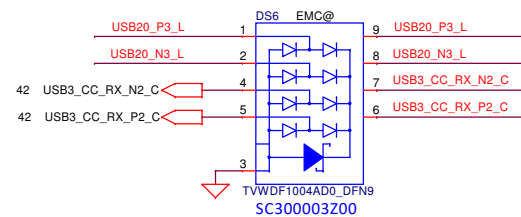
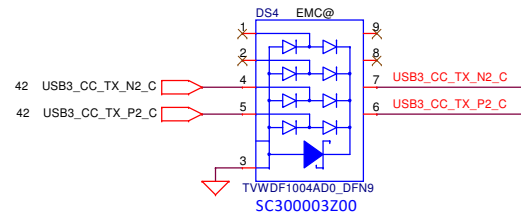
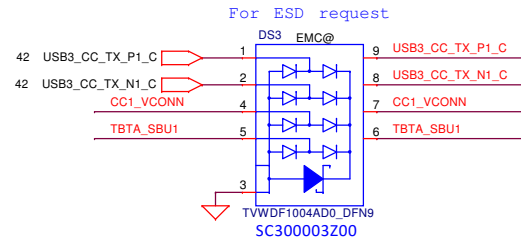
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SILERGY SY6861B1 MOS Current Limit				
TYPEC_1P5A	TYPEC_3A	RSET(kΩ)	MODE	limit point
L	L	6.2	0.9A	1.09A
L	H	3.53	1.5A	1.92A
H	L	2.54	2A	2.67A
*H	H	1.94	3A	3.5A

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CC1_VCONN & CC2_VCONN need 20mil trace width.

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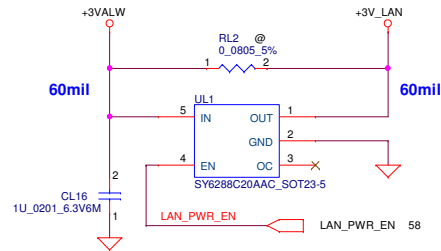
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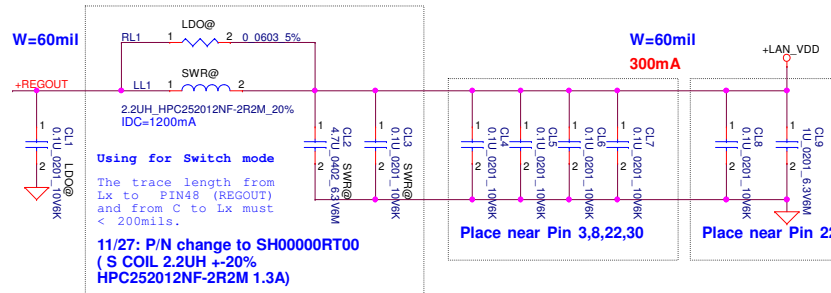
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+3V_LAN Rising time (10%-90%) must >0.5mS and <100mS

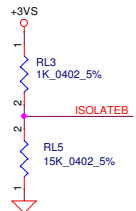
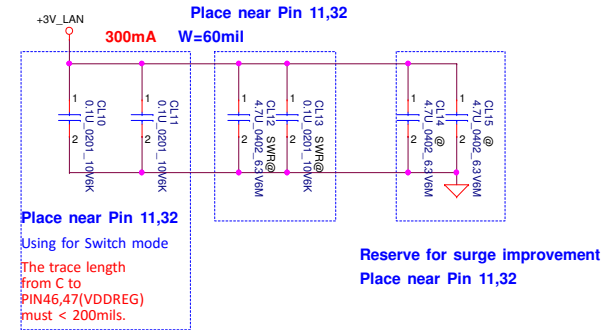


From EC
High active.
EN threshold voltage min:1.2V
typ:1.6V max:2.0V
Current limit threshold 1.5~2.8A
+3V_LAN Rising time must >0.5ms and <100ms

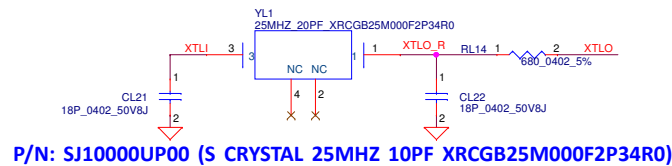
RTL8111H LDO mode
RTL8118ASA SWR mode



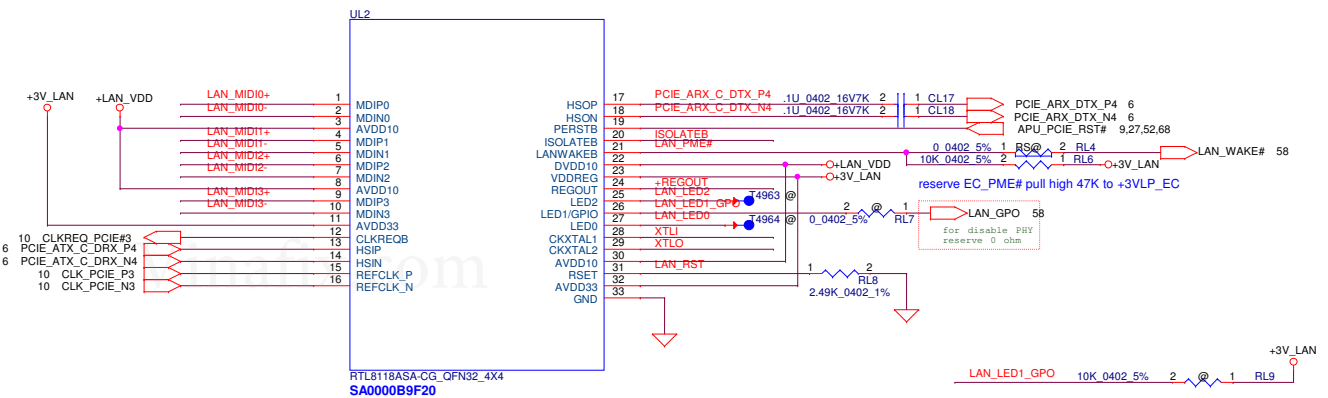
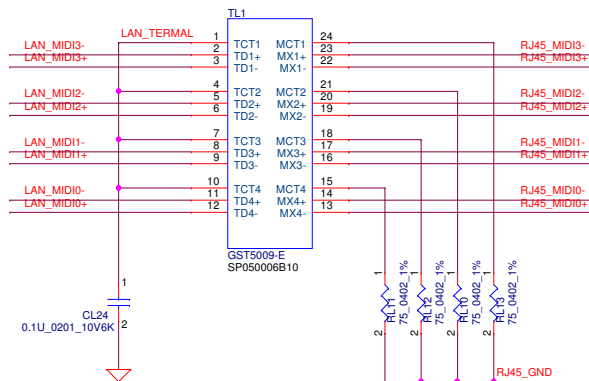
11/27: P/N change to SH00000RT00
(S COIL 2.2UH +20%
HPC252012NF-2R2M 1.3A)



LAN_CLKREQ# pull up at PCH side

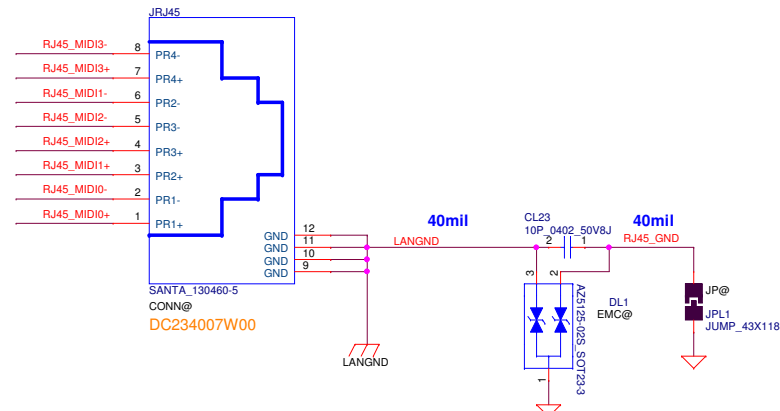


P/N: SJ10000UP00 (S CRYSTAL 25MHZ 10PF XRCGB25M000F2P34R0)



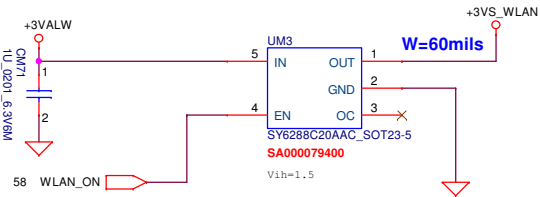
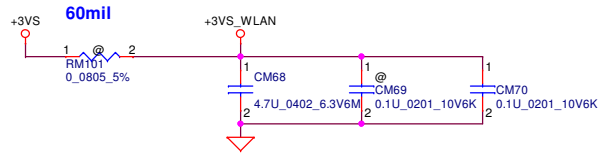
SA0000B9F20, S IC RTL8118ASA-CG QFN 32P E-LAN CTRL

LAN Connector



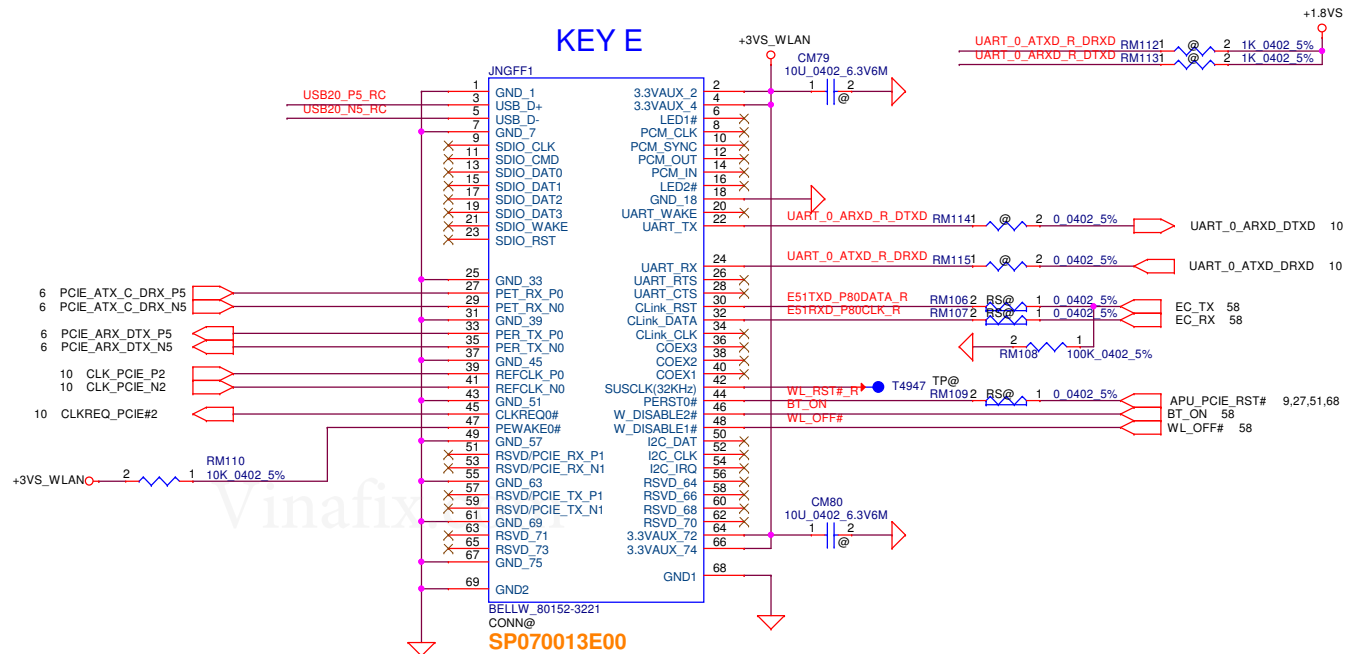
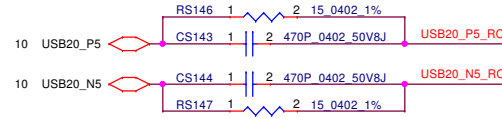
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Wireless LAN



NGFF WL+BT (KEY E)

74	3.3v	GND	75
72	3.3v	RESERVED/REFCLKN1	73
70	UM_Power_SRC/GPIO/PWVWake1#	RESERVED/REFCLKP1	71
68	UM_Power_SNK/CLKREQ1#	GND	69
66	UM_SWP/PERST1#	Reserved/PERn1	67
64	RESERVED	Reserved/PERp1	65
62	ALERTA [I/O](0.3.3v)	GND	63
60	QC CLK [I/O](0.3.3v)	Reserved/PETn1	61
58	QC DATA [I/O](0.3.3v)	Reserved/PETp1	59
56	W_DISABLE1 [O](0.3.3v)	GND	57
54	Reserved_W_DISABLE1 [O](0.3.3v)	PWVWake1 [O](0.3.3v)	55
52	PERST0W [I/O](0.3.3v)	CLKREQ0n [O](0.3.3v)	53
50	SUSCLK32MHz [O](0.3.3v)	GND	51
48	CODE1 [I/O](0.1.8v)	REFCLKIN0	49
46	CODE2 [O](0.1.8v)	REFCLKP0	47
44	CODE3 [O](0.1.8v)	GND	45
42	VENDOR DEFINED	PERn0	43
40	VENDOR DEFINED	PERp0	41
38	VENDOR DEFINED	GND	39
36	UART RTS [O](0.1.8v)	PETn0	37
34	UART CTS [I/O](0.1.8v)	PETp0	35
32	UART Tx [O](0.1.8v)	GND	33
	CODE4 [I/O](0.1.8v)	PERn10n [I/O](0.1.8v)	
	CODE5 [I/O](0.1.8v)	PERp10n [I/O](0.1.8v)	
	CODE6 [I/O](0.1.8v)	PERn10p [I/O](0.1.8v)	
	CODE7 [I/O](0.1.8v)	PERp10p [I/O](0.1.8v)	
22	UART Rx [I/O](0.1.8v)	SDIO Reset [O](0.0.1.8v)	23
20	UART Wakeup [I/O](0.3.3v)	SDIO Wakeup [I/O](0.3.3v)	21
18	GND	SDIO DATA [I/O](0.1.8v)	19
16	LED#1 [I/O](0.1.8v)	SDIO DATAn [I/O](0.1.8v)	17
14	PCM_OUT/ISD_S_OUT [O](0.1.8v)	SDIO DATAp [I/O](0.1.8v)	15
12	PCM_IN/ISD_S_IN [O](0.1.8v)	SDIO DATA [I/O](0.1.8v)	13
10	PCM_SYNC/ISD_WS [O](0.1.8v)	SDIO CMDn [O](0.1.8v)	11
8	PCM_CLK/ISD_SCK [O](0.1.8v)	SDIO CLK [O](0.1.8v)	9
6	LED#1 [I/O](0.1.8v)	GND	7
4	3.3v	USB_D+	5
2	3.3v	USB_D-	3
		GND	1



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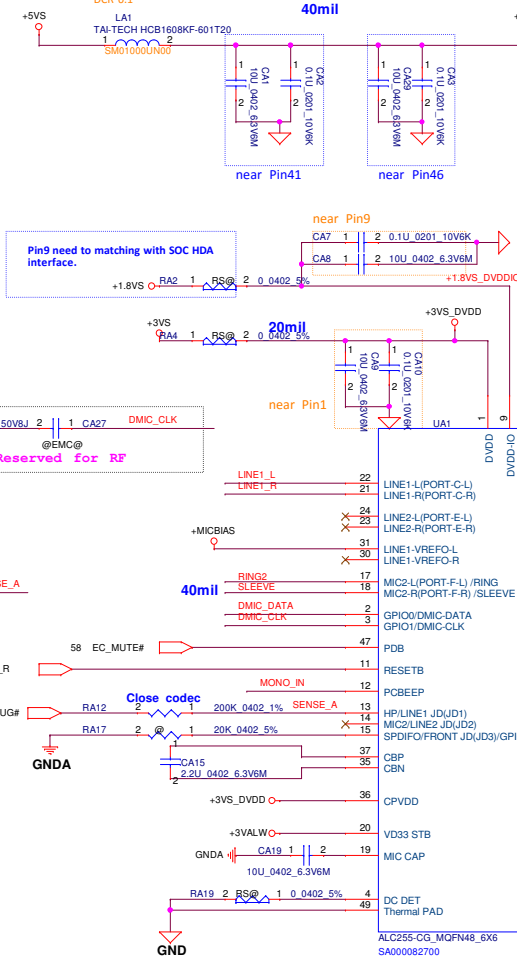
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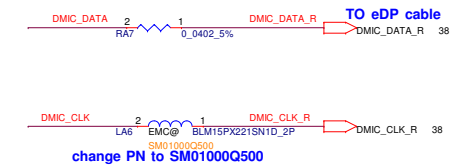
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2000mA 600ohm@100MHz
DCR 0.1



MIC BOM upload by Audio Team



The schematic diagram illustrates the IOB section of the SC5BAT54100. It features several input and output pins connected to various components:

- MIC2_VREF0**: Connected to RA15 (2.2K 0402 5%) and RA18 (2.2K 0402 5%).
- MICBIAS**: Connected to DA3, which is part of a differential pair (RA23, RA28) with 4.7K 0402 5% resistors.
- HP_LEFT**: Connected to RA20 (2 0.0603 5%) and HPOUT_L_1.
- HP_RIGHT**: Connected to RA21 (2 0.0603 5%) and HPOUT_R_1.
- LINE1_L**: Connected to CA23 (2 4.7U 0402 6.3V6M) and LINE1_L.
- LINE1_R**: Connected to CA24 (2 4.7U 0402 6.3V6M) and LINE1_R.
- SLEEVE**: Connected to RA15 and RA18.
- RING2**: Connected to RA15 and RA18.

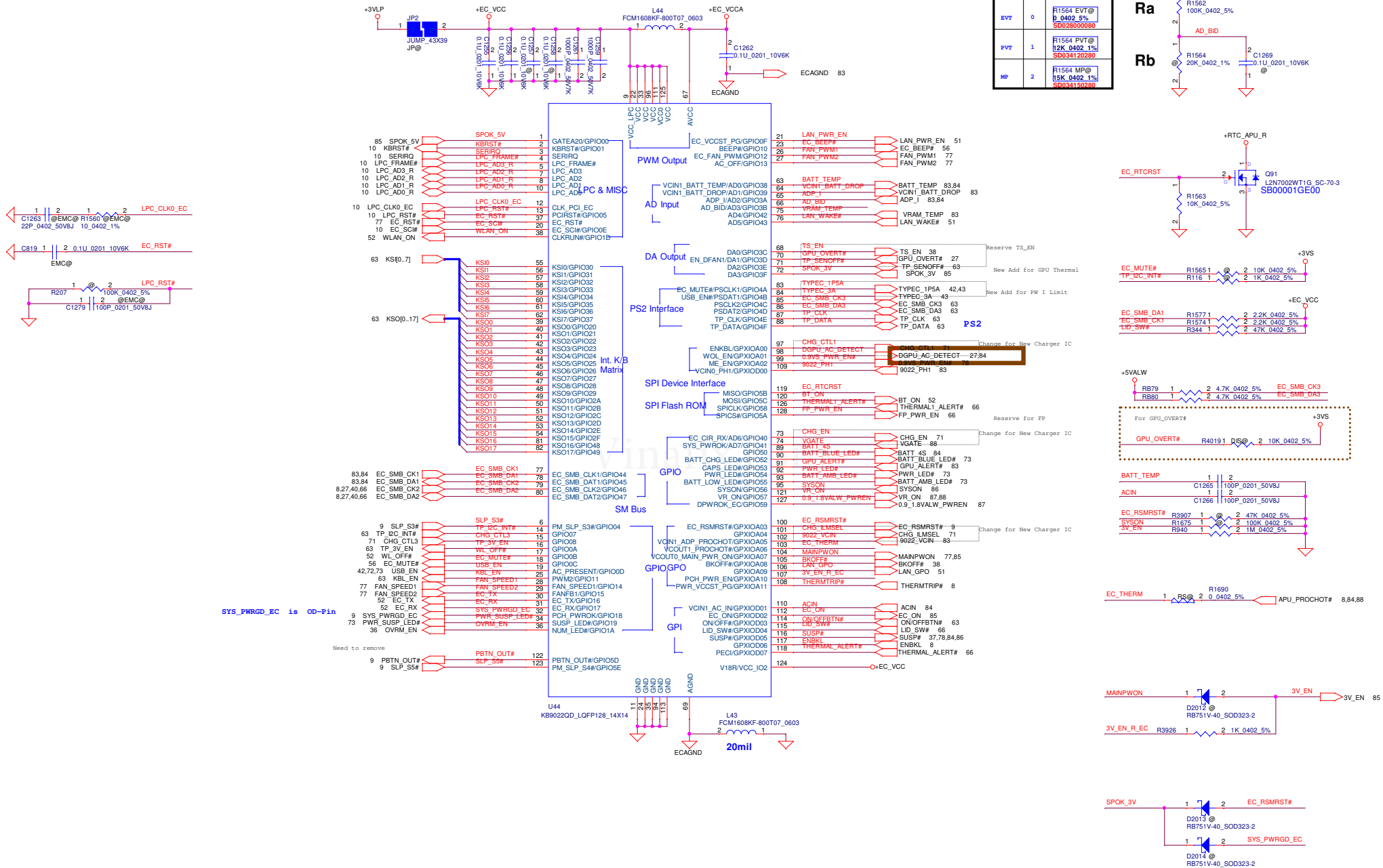
The components are labeled with their values and footprints: RA15 (2.2K 0402 5%), RA18 (2.2K 0402 5%), RA20 (2 0.0603 5%), RA21 (2 0.0603 5%), CA23 (2 4.7U 0402 6.3V6M), CA24 (2 4.7U 0402 6.3V6M), DA3, RA23 (4.7K 0402 5%), and RA28 (4.7K 0402 5%).

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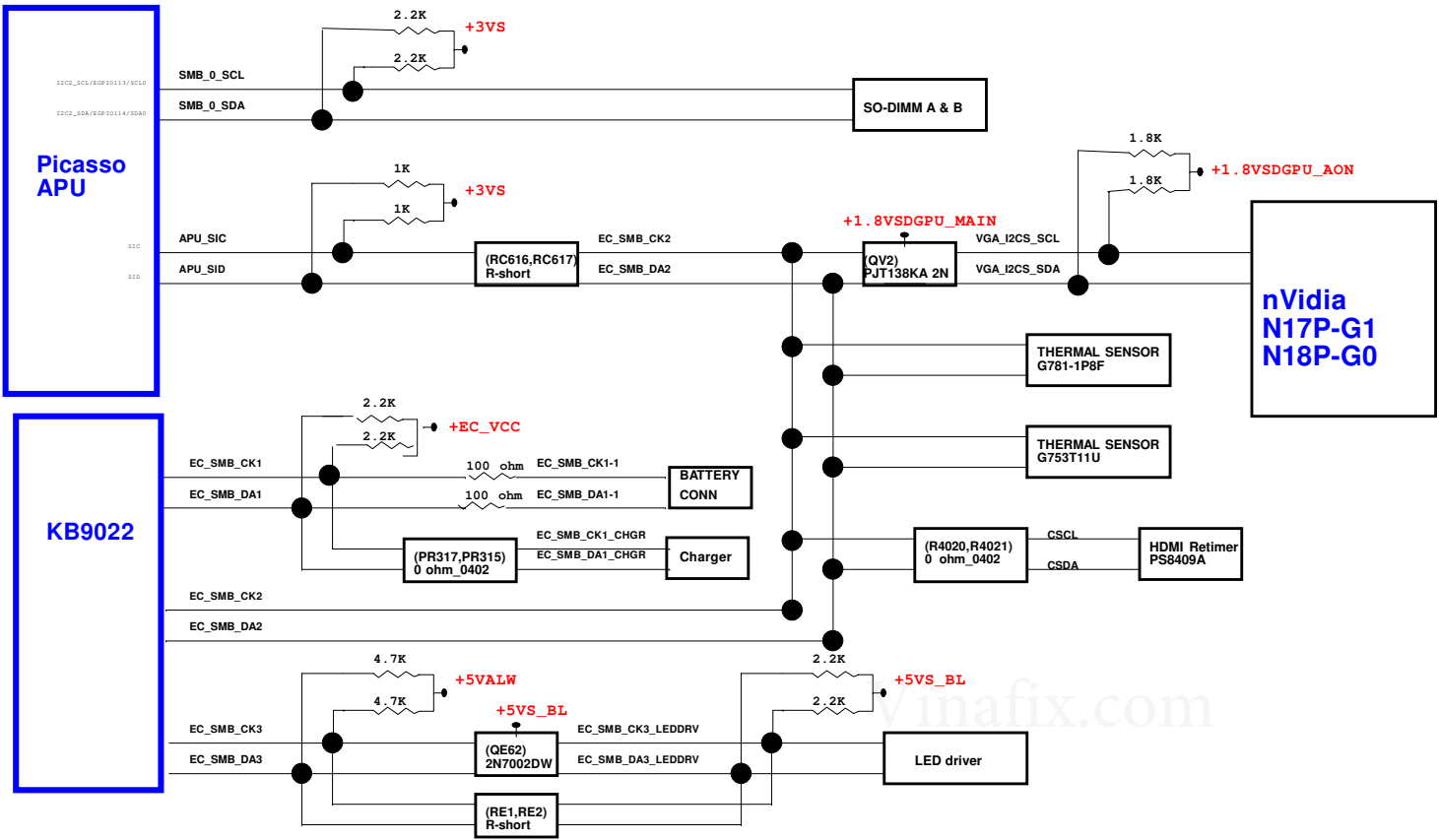
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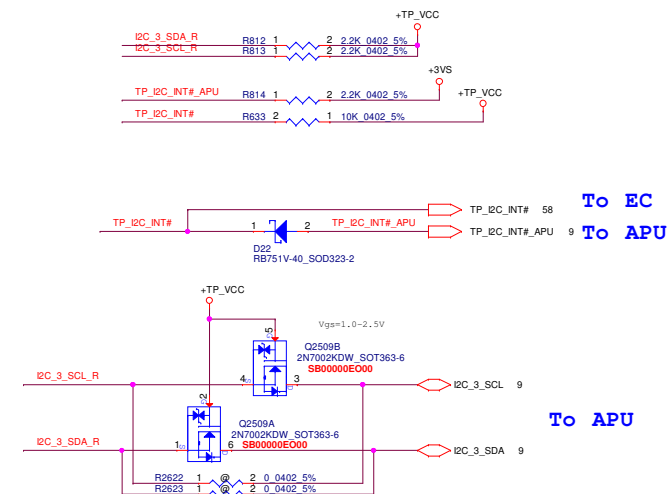
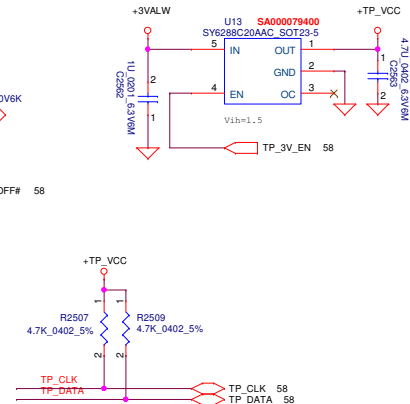
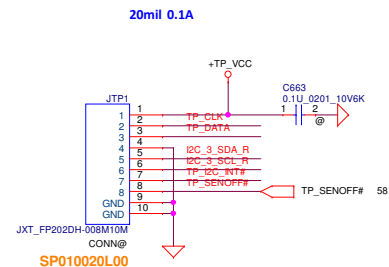
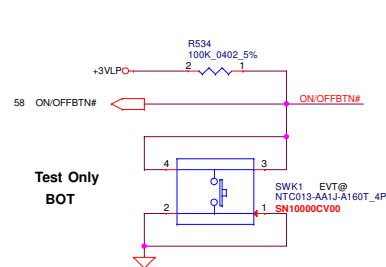


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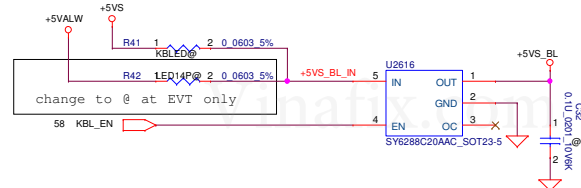
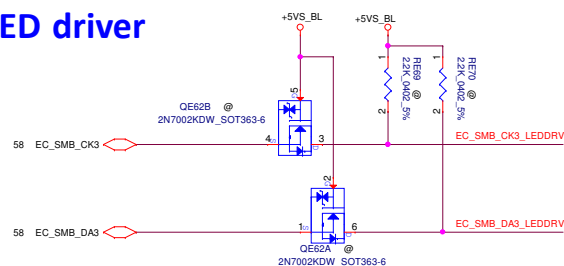
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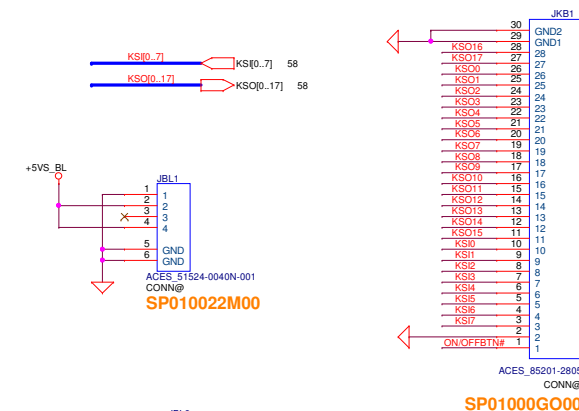
TP/B Conn.



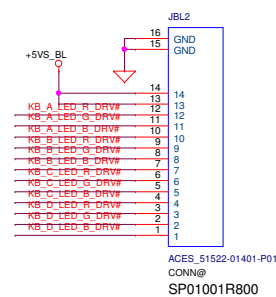
LED driver



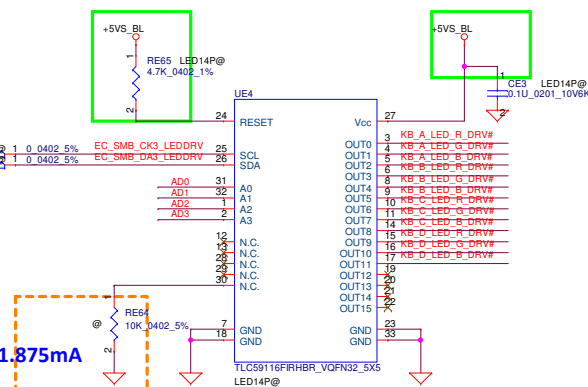
KB Conn. / Backlight



KB Conn.
KB BackLight



set RE7 to 10k / output = 1.875mA



Raptor: NC for 59116F

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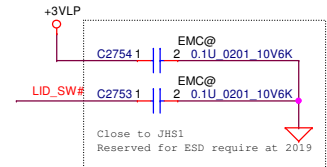
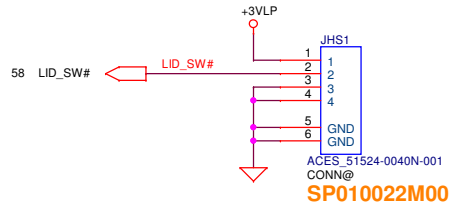
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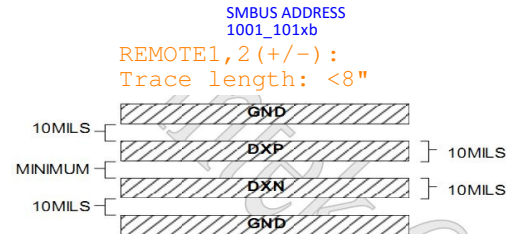
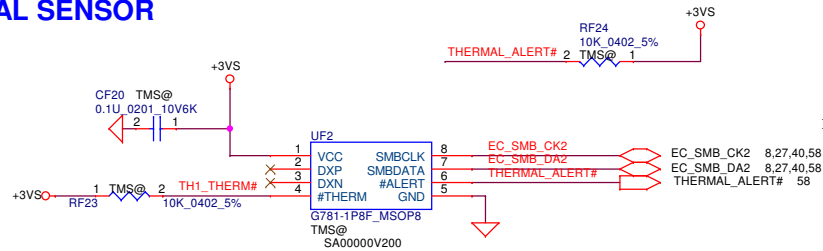
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To Hall sensor/B



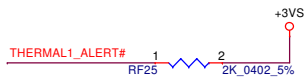
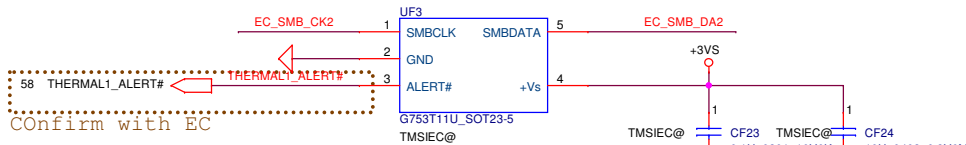
THERMAL SENSOR



Slave Address
The G781 appears to the SMBus as one device having a common address for both ADC channels.
The G781 and G781-1 have the following SMBus slave address:

	A6	A5	A4	A3	A2	A1	A0
G781	1	0	0	1	1	0	0
G781-1	1	0	0	1	1	0	1

THERMAL SENSOR IEC safety



Nuvoton NCT7717U SA00005NN00
GMT G753T11U SA00008CH00

ALERT# point hardware power-on setting
The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin:

PULL-UP RESISTOR	TEMPERATURE (°C)
2kΩ	75
7.5kΩ	90
10.5kΩ	100
14kΩ	105
18.7kΩ	110

6.3 Address Setting
NCT7717U I²C/ SMBus™ address is 1001000xb (x is R/W bit).

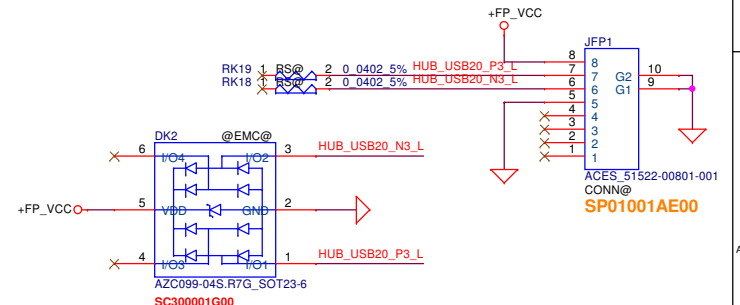
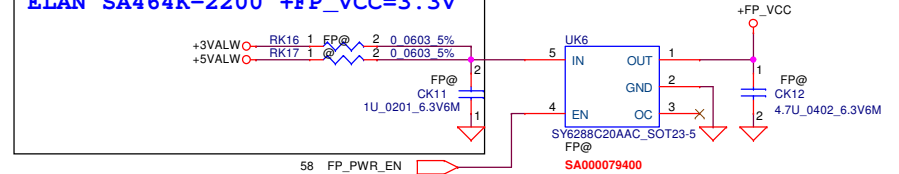
Slave Address
The G753 appears to the SMBus as one device having a common address for both ADC channels.
The G753 has the following SMBus slave address:

	A6	A5	A4	A3	A2	A1	A0
G753	1	0	0	1	0	0	0

The G753 also responds to the SMBus Alert Response slave address (see the Alert Response Address section).

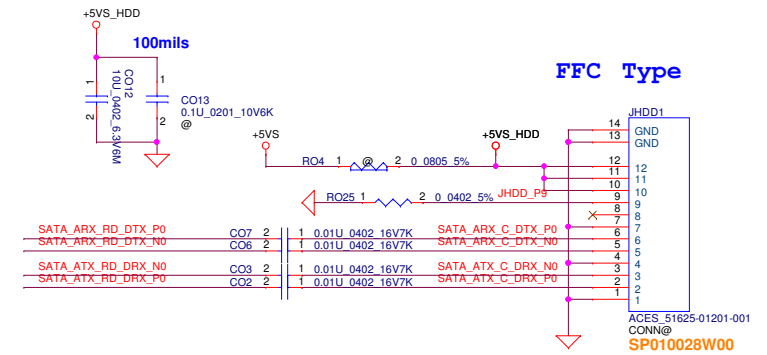
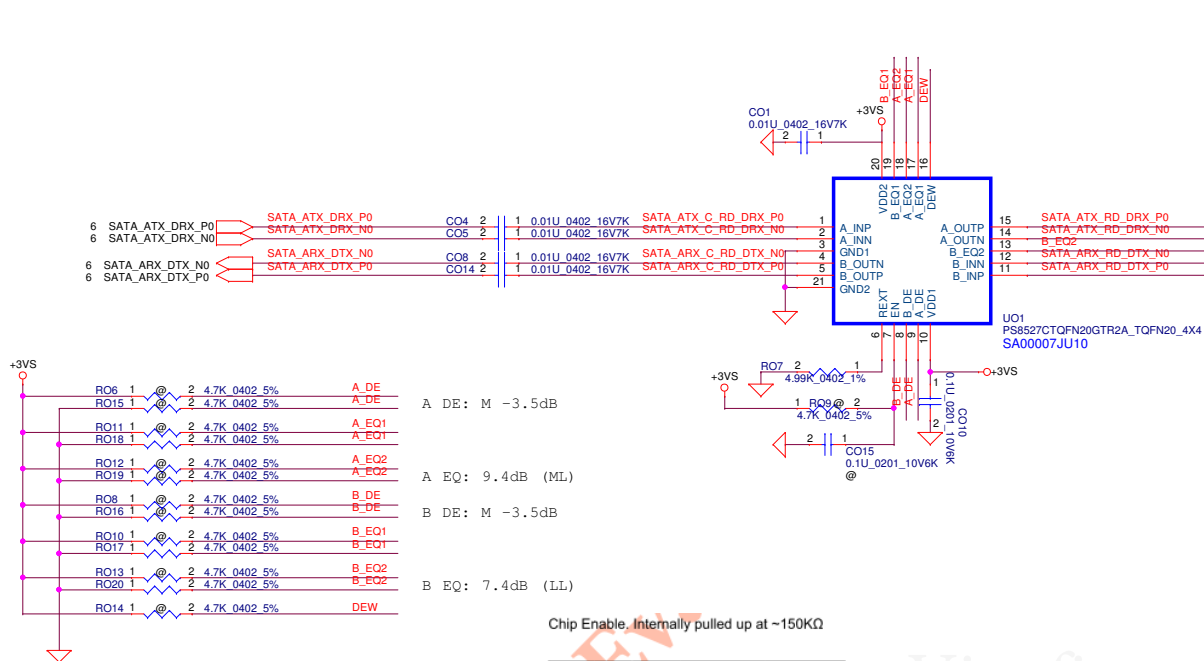
Finger Print

Power Source Check
EGIS ETU801 +FP_VCC=5V
ELAN SA464K-2200 +FP_VCC=3.3V



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SATA Re-Driver and cable HDD Conn.



EN	Status
L	Chip disabled
H	Chip enabled(default)

Programmable output de-emphasis level setting for channel A.
Internally tied to VDD/2(M status).

A _{DE}	De _{Emphasis}
M	-3.5dB(Default)
L	0dB
H	-6dB

Programmable output de-emphasis level setting for channel B.
Internally tied to VDD/2(M status).

B_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Equalizer control and program for channel A.
Internally tied to VDD/2 (M status).

A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

Equalizer control and program for channel B.
Internally tied to VDD/2(M status).

B_EQ2	B_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

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								Date:					

3VS

RM1261 2 4.7K 0402 5% A2_DE

RM1201 2 4.7K 0402 5% A2_DE

RM1291 2 4.7K 0402 5% A2_EQ1

RM1231 2 4.7K 0402 5% A2_EQ1

RM1301 2 4.7K 0402 5% A2_EQ2

RM1241 2 4.7K 0402 5% A2_EQ2

RM1271 2 4.7K 0402 5% B2_DE

RM1211 2 4.7K 0402 5% B2_DE

RM1281 2 4.7K 0402 5% B2_EQ1

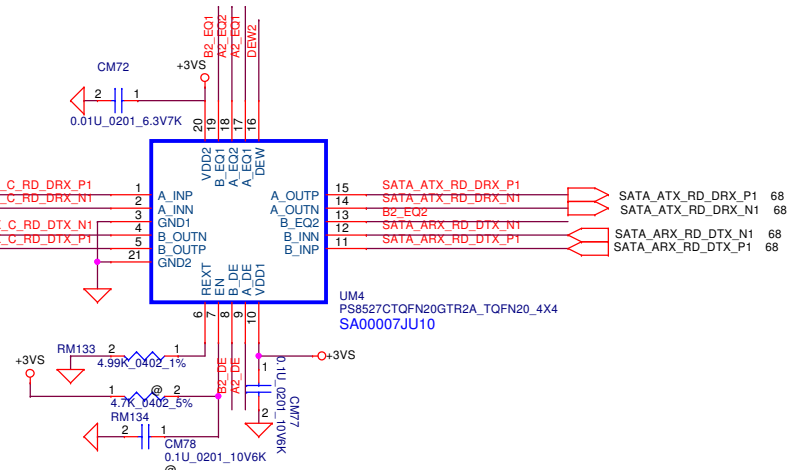
RM1221 2 4.7K 0402 5% B2_EQ1

RM1311 2 4.7K 0402 5% B2_EQ2

RM1251 2 4.7K 0402 5% B2_EQ2

RM1321 2 4.7K 0402 5% DEW2

Ground symbol



B EQ: 2.4dB (LM)

Chip Enable. Internally pulled up at $\sim 150\text{K}\Omega$

EN	Status
L	Chip disabled
H	Chip enabled(default)

A_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

B_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

B_EQ2	B_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

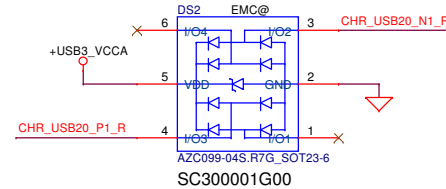
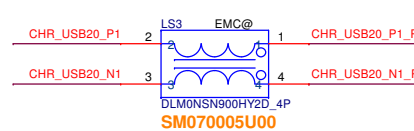
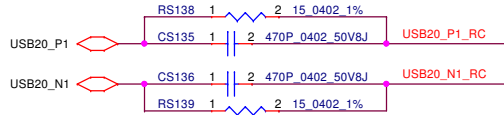
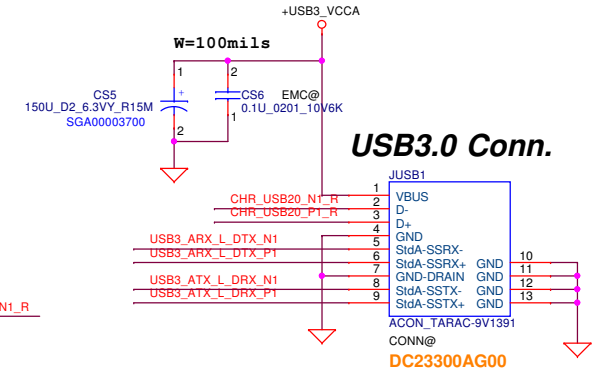
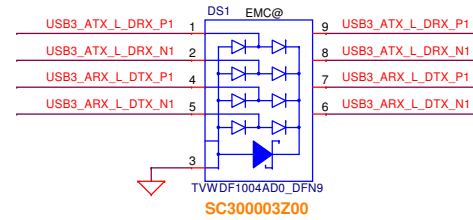
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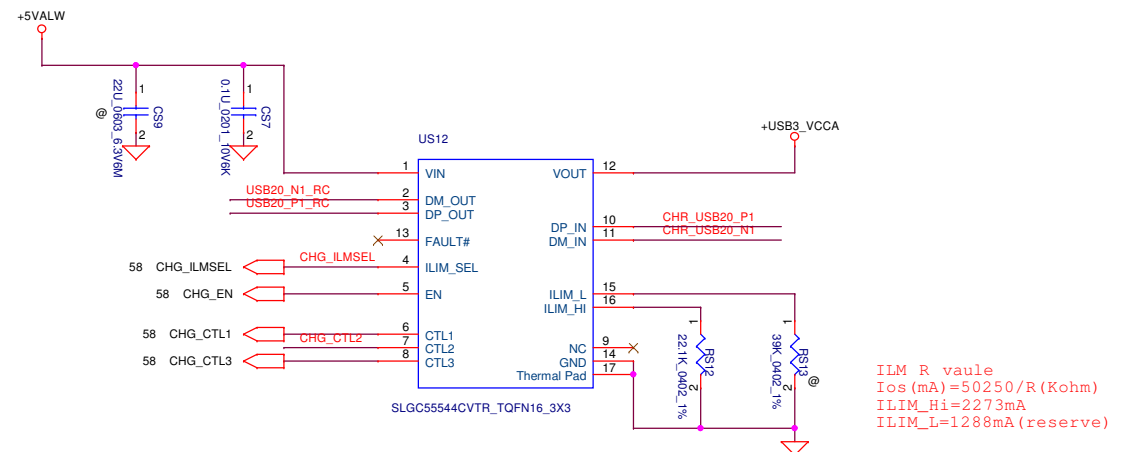
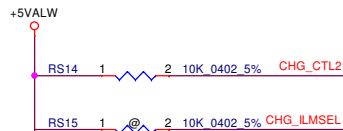
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USB3.0



USB Host Charger



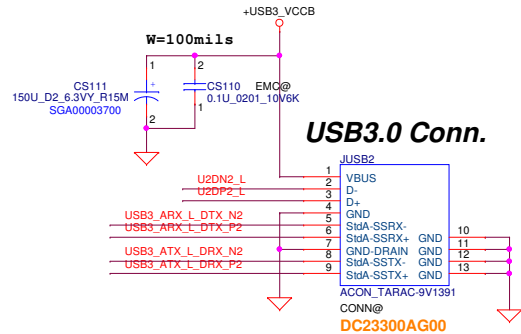
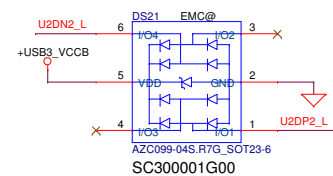
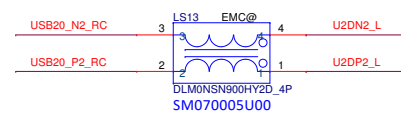
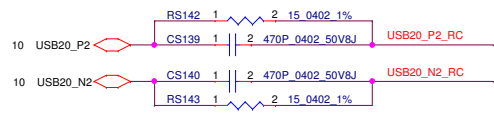
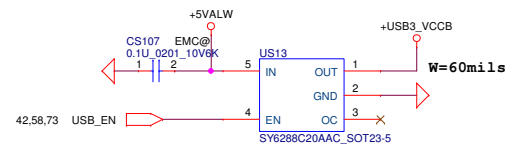
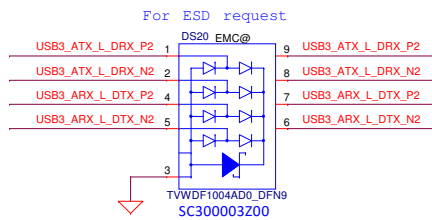
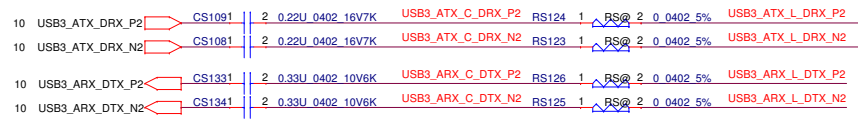
USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Setting	Limit	Note
0	0	1	0	1	SDP1-OFF	ILIM_H		Port power off
1	0	1	0	1	SDP1	ILIM_H		Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H		Data Lines Disconnected
1	1	1	1	1	CDP	ILIM_H		Data Lines Connected

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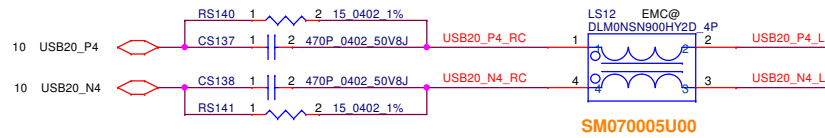
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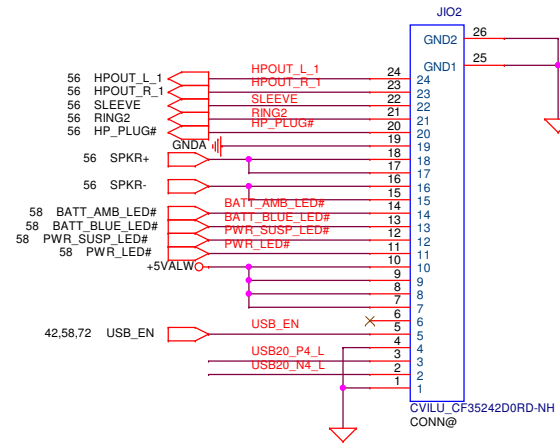
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IO/B CONN



SM070005U00



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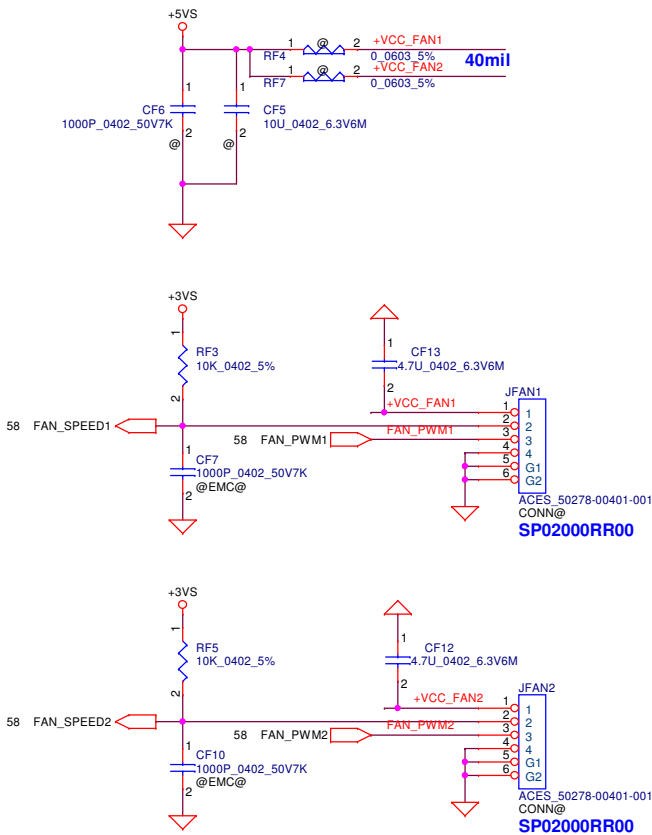
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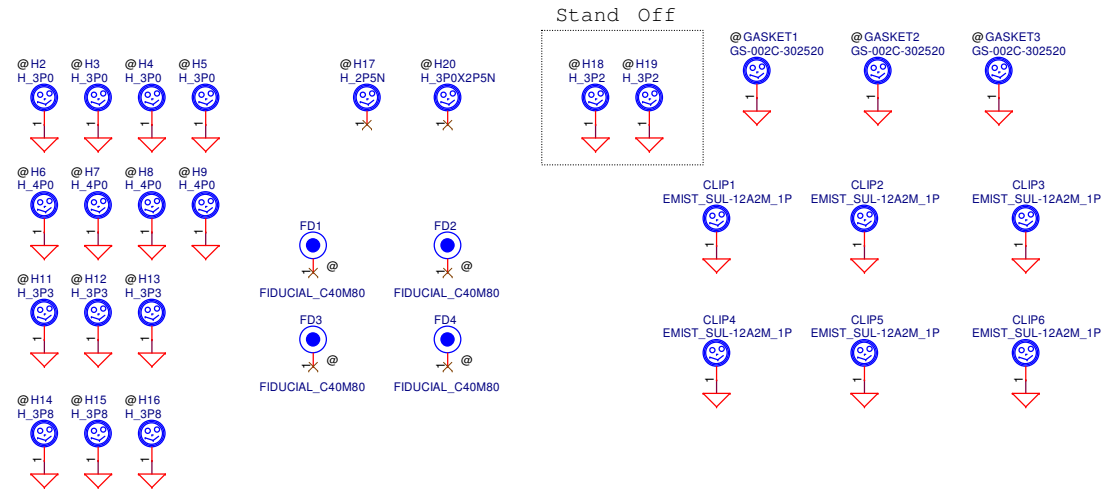
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FAN Conn



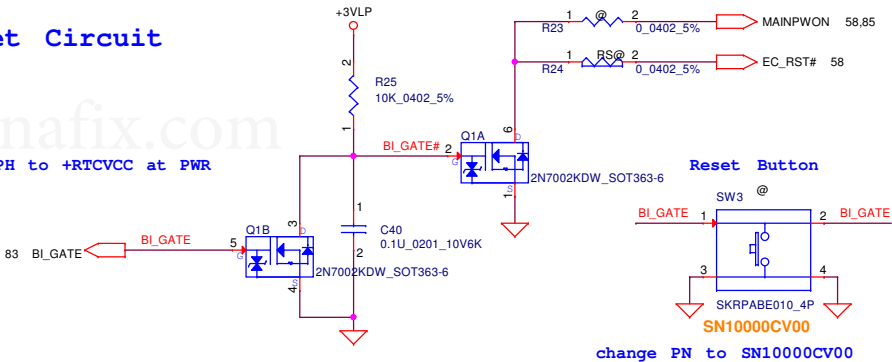
Screw Hole



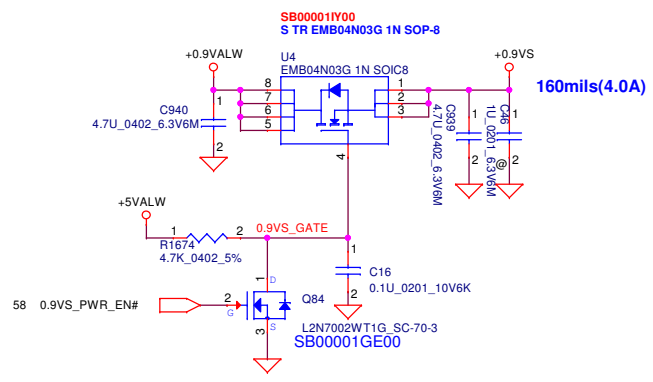
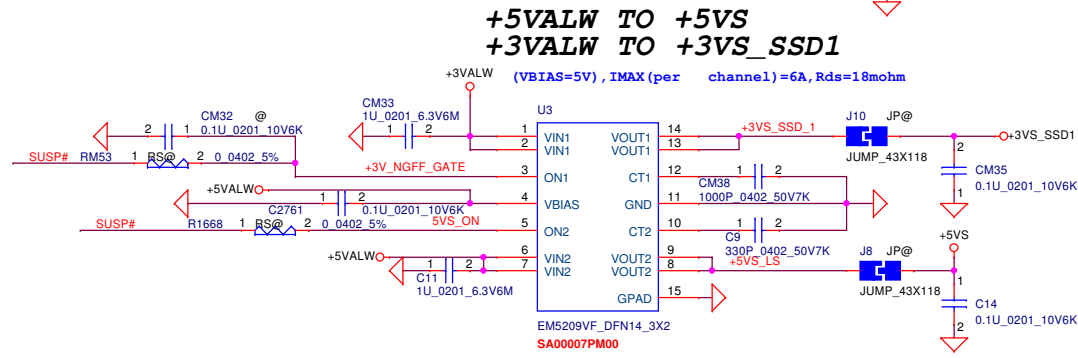
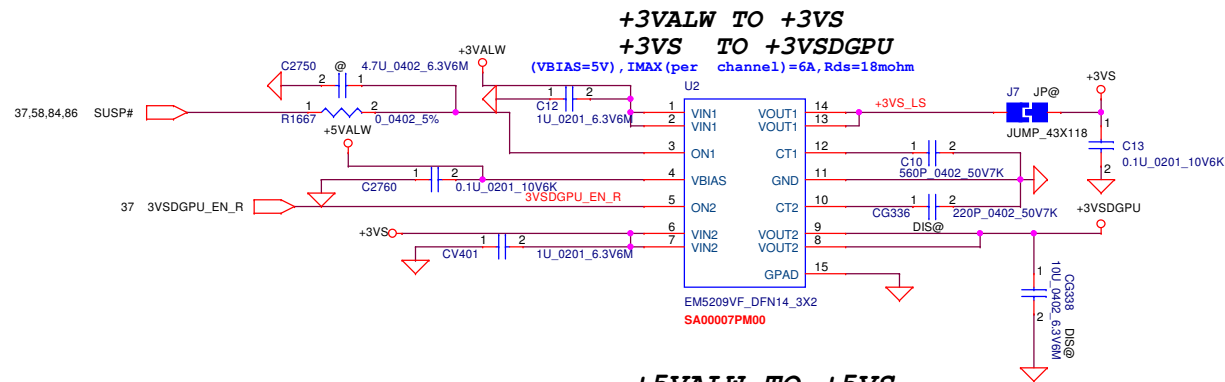
Reset Circuit

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BI_GATE PH to +RTCVCC at PWR side



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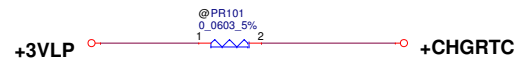
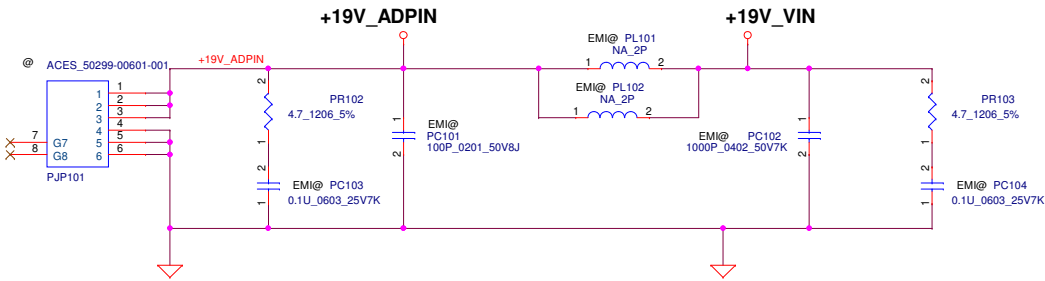
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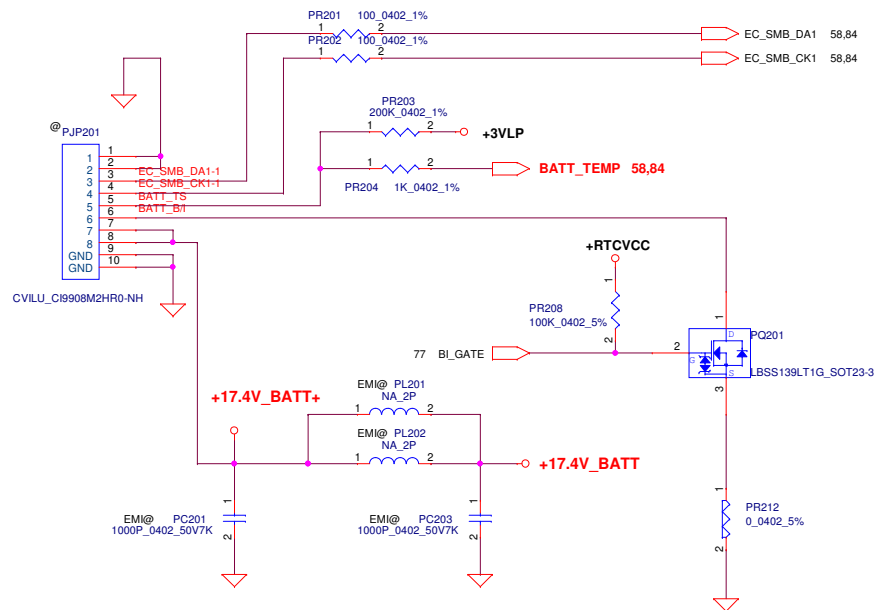
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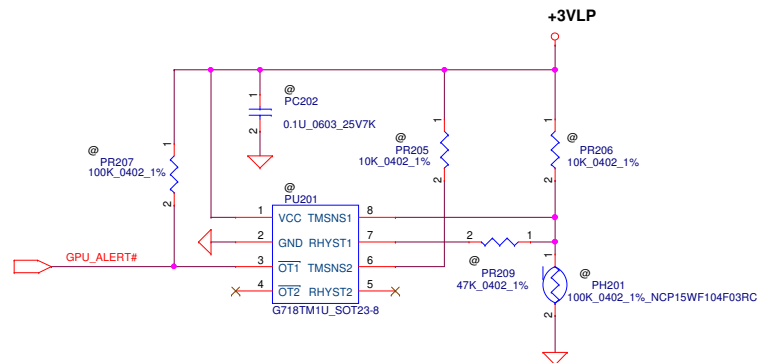


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58 GPU_ALERT#



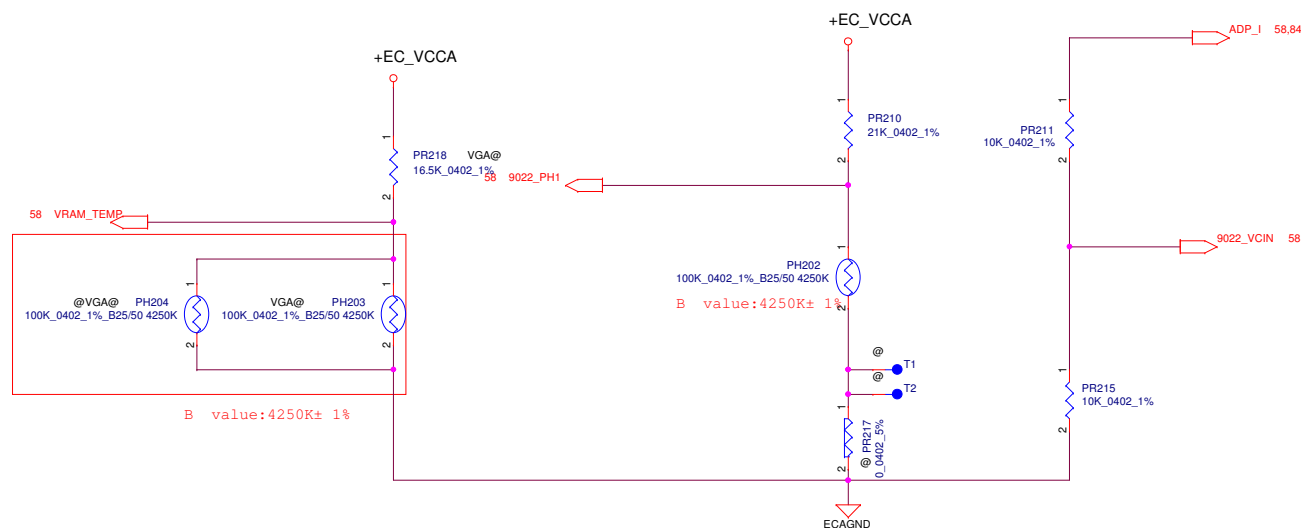
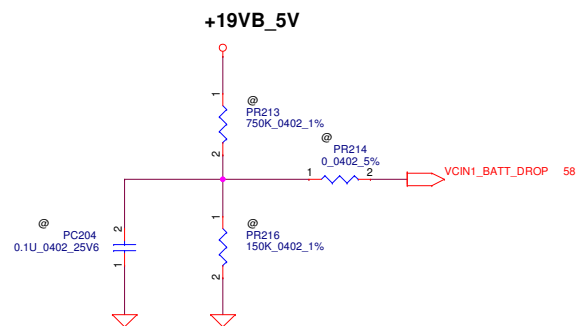
For KB9022 OTP	Active	Recovery
VCIN0_PH (V)	85C, 1V	50C, 2V
PH202 (ohm)	9.1831K	33.19K

For KB9022	Active	Recovery
ADP_I	96%, 1.3286V	85%, 1.1764V
9022_Vcin	150%, 1.038V	150%, 1.038V

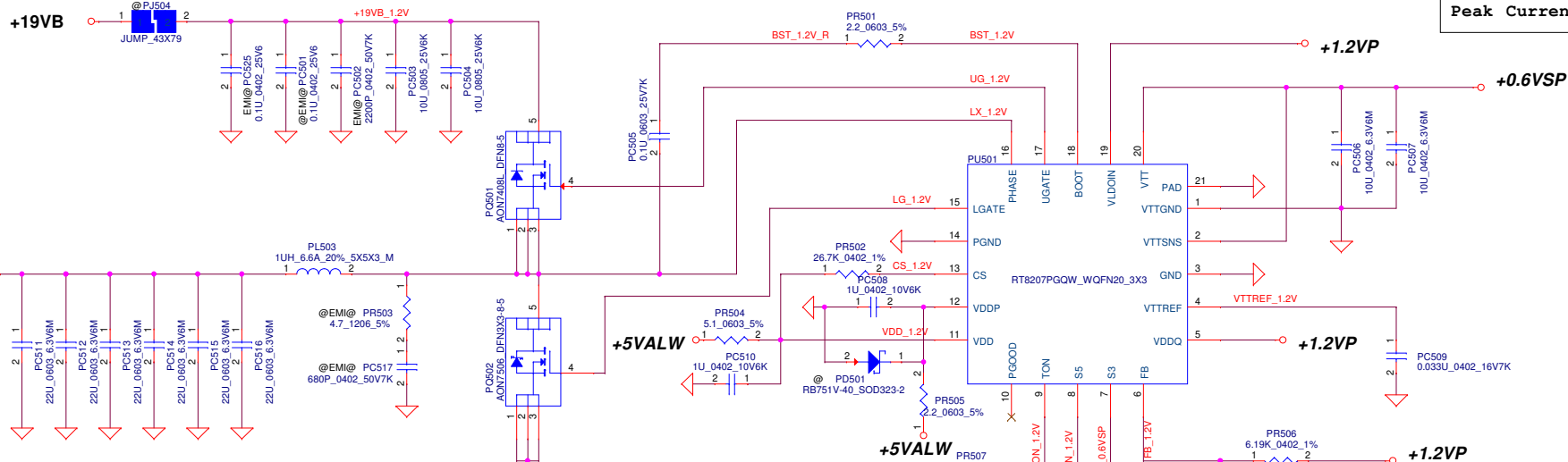
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2013/10/02
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

Reserve for 2-cell design



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0.6Volt +/- 5%
TDC 0.7A
Peak Current 1A

Mode	Level	+0.6VSP	VTTREF_1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

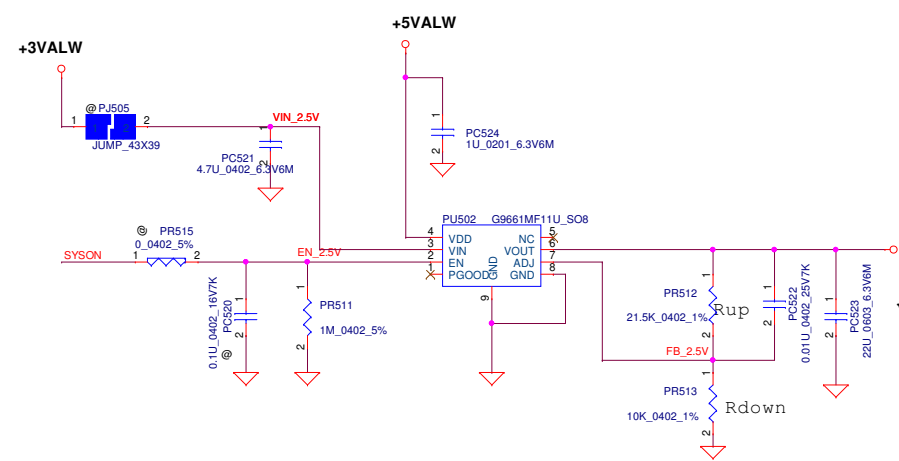
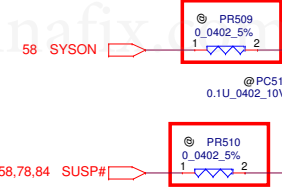
Note: S3 - sleep ; S5 - power off

H/S AON7408 Rds(on) : typ:27mOhm, max:34mOhm
Idsm(TA=25)=7.5A, Idsm(TA=70)=5.5A

L/S AON7506 Rds(on) : typ:13mOhm, max:15.8mOhm
Idsm(TA=25)=12A, Idsm(TA=70)=10.5A

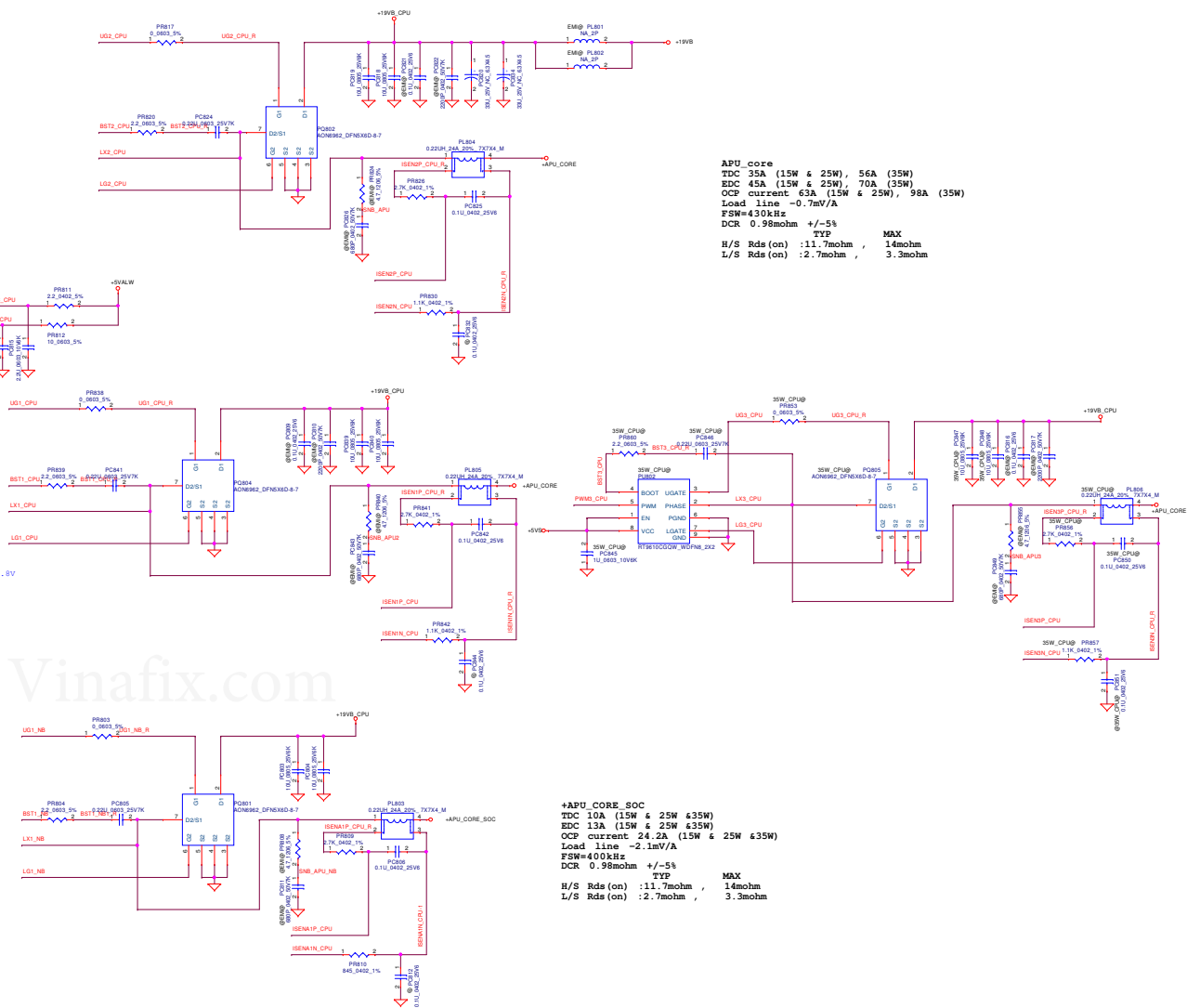
Choke: 5x5x3
Rdc=13mohm(Typ), 14mohm(Max)

Switching Frequency: 530kHz
Ipeak=10.91A
Iocp~120%
OVP: 110%~120%



$$V_{out} = 0.8V * (1 + (21.5/10)) = 2.52V \quad 0.8\%$$

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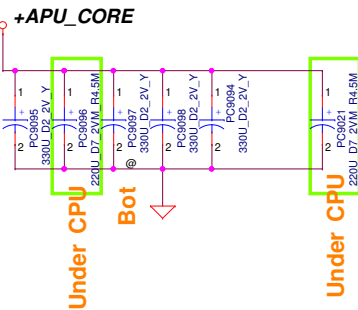
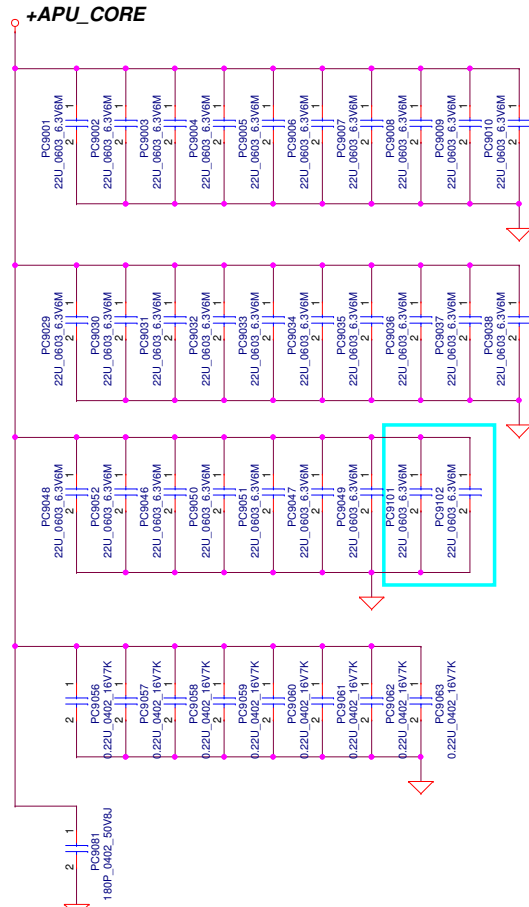
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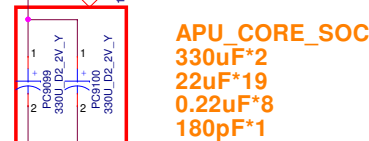
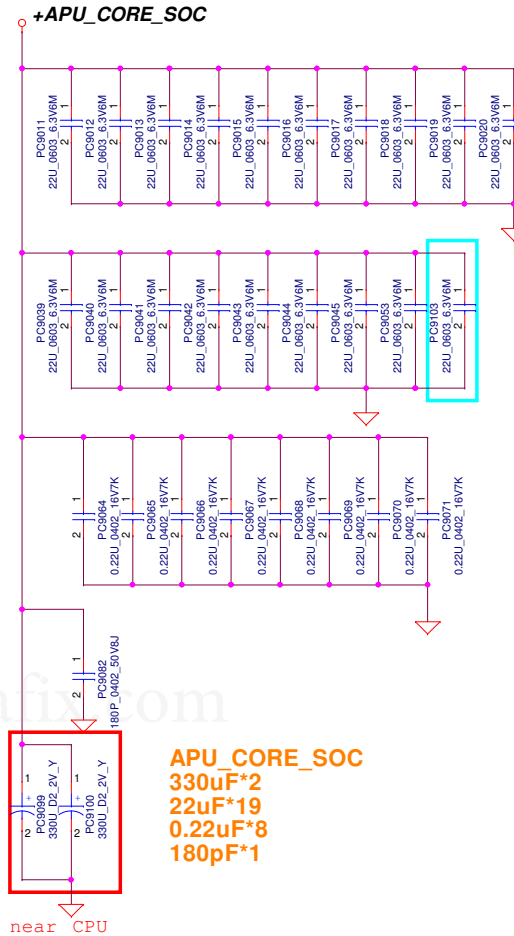
+APU_CORE



APU_CORE
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220uF*2
22uF*29
0.22uF*8
180pF*1

330u is common part SGA00009S00

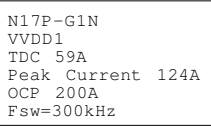
+APU_CORE_SOC



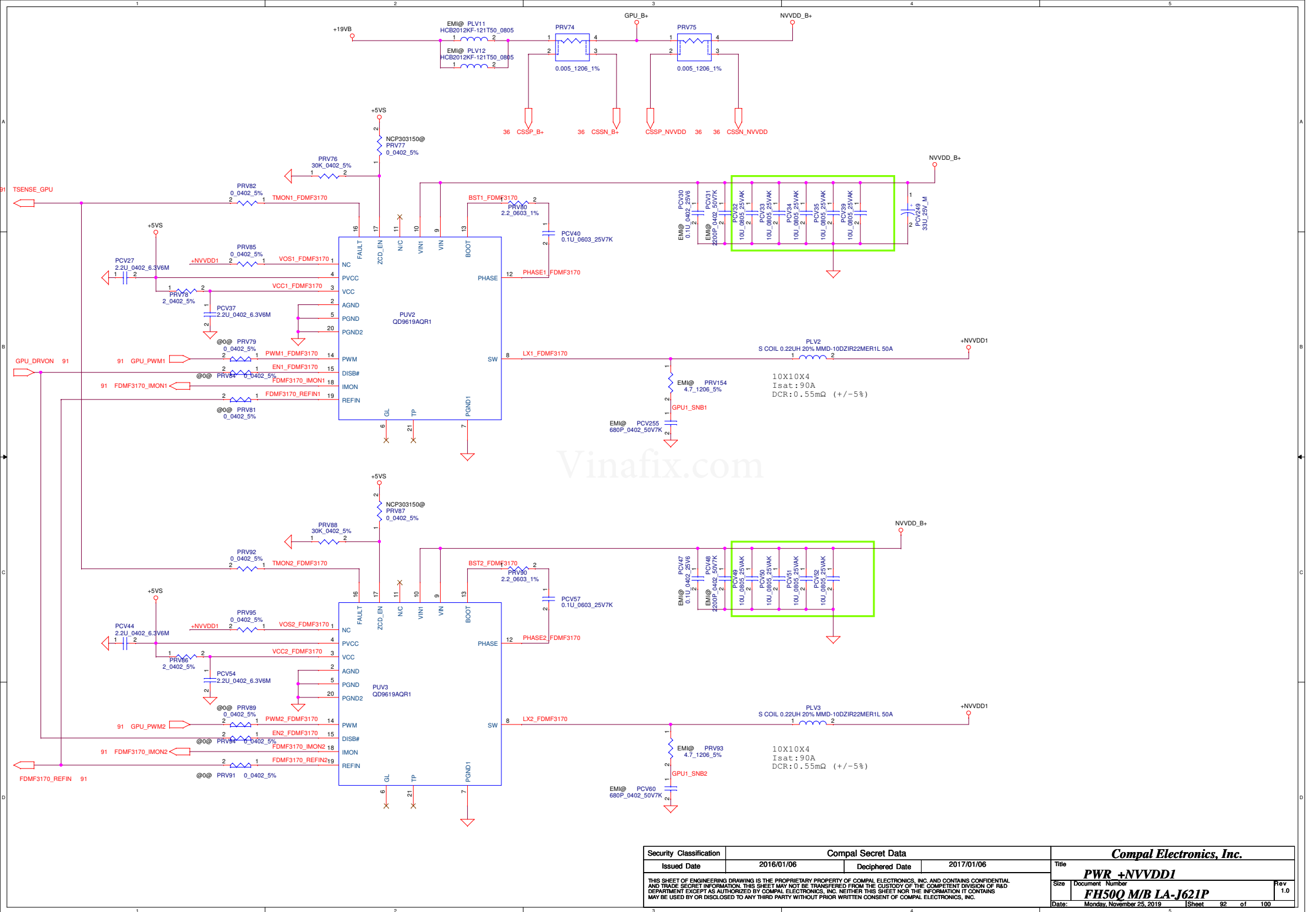
APU_CORE_SOC
330uF*2
22uF*19
0.22uF*8
180pF*1

330u is common part SGA00009S00

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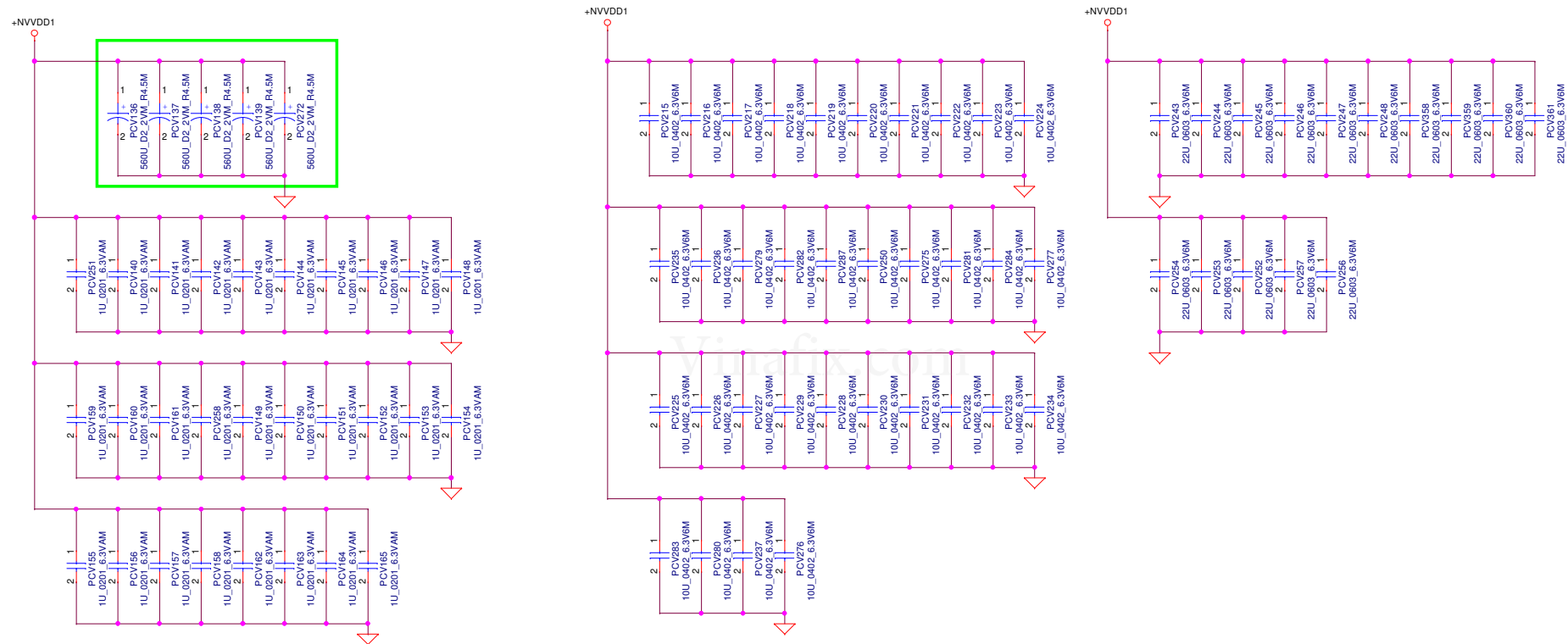


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				FH500 M/B LA-J621P	

Table 5.11 GB4D-128 Package: Power Rail Filtering

Rail (GPU Ball)	Balls	Voltage	Filtering under GPU	Filtering Near GPU
GB4D-128 Package				
NVVDD		Varies	26 x 0.47uF (0201W X6S) 34 x 10uF (0603 X6S) Alternate solution: 13 x 1uF (0402 or 0201W, X6S) ³ 34 x 10uF (0603 X6S)	15 x 22uF (0805 X6S)

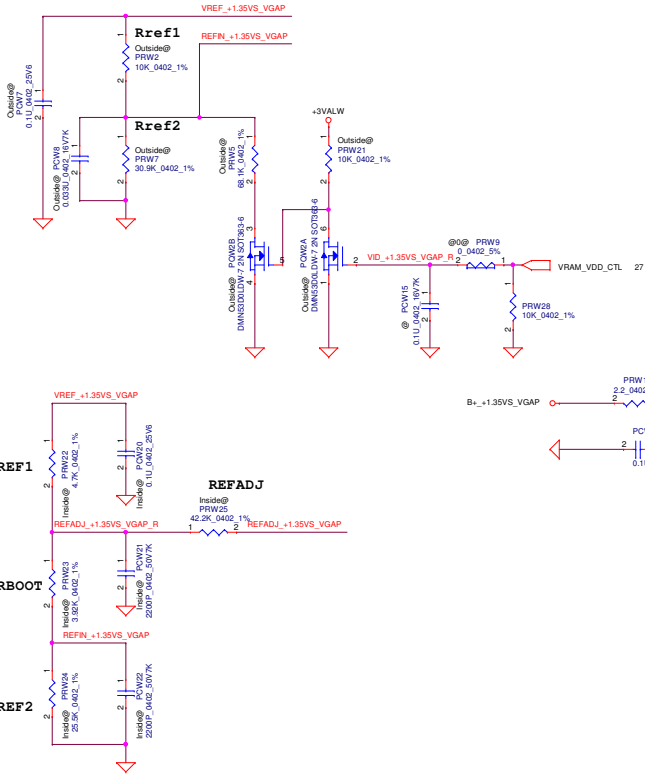
N18P-G0
+NVVDD
560uF X 5
22uF_0603 X 15
10uF_0402 X 34
1uF_0201 X 28



Micron & Hynix & Samesung VRAM
 $V_{boot} = V_{ref} \cdot R2 / (R1 + R2 + 80)$

When, VRAM_VDD_CTL=High
 $V_{boot} = 2 \cdot 30.9K / (10K + 30.9K + 80) = 1.508V \quad (x1.11)$

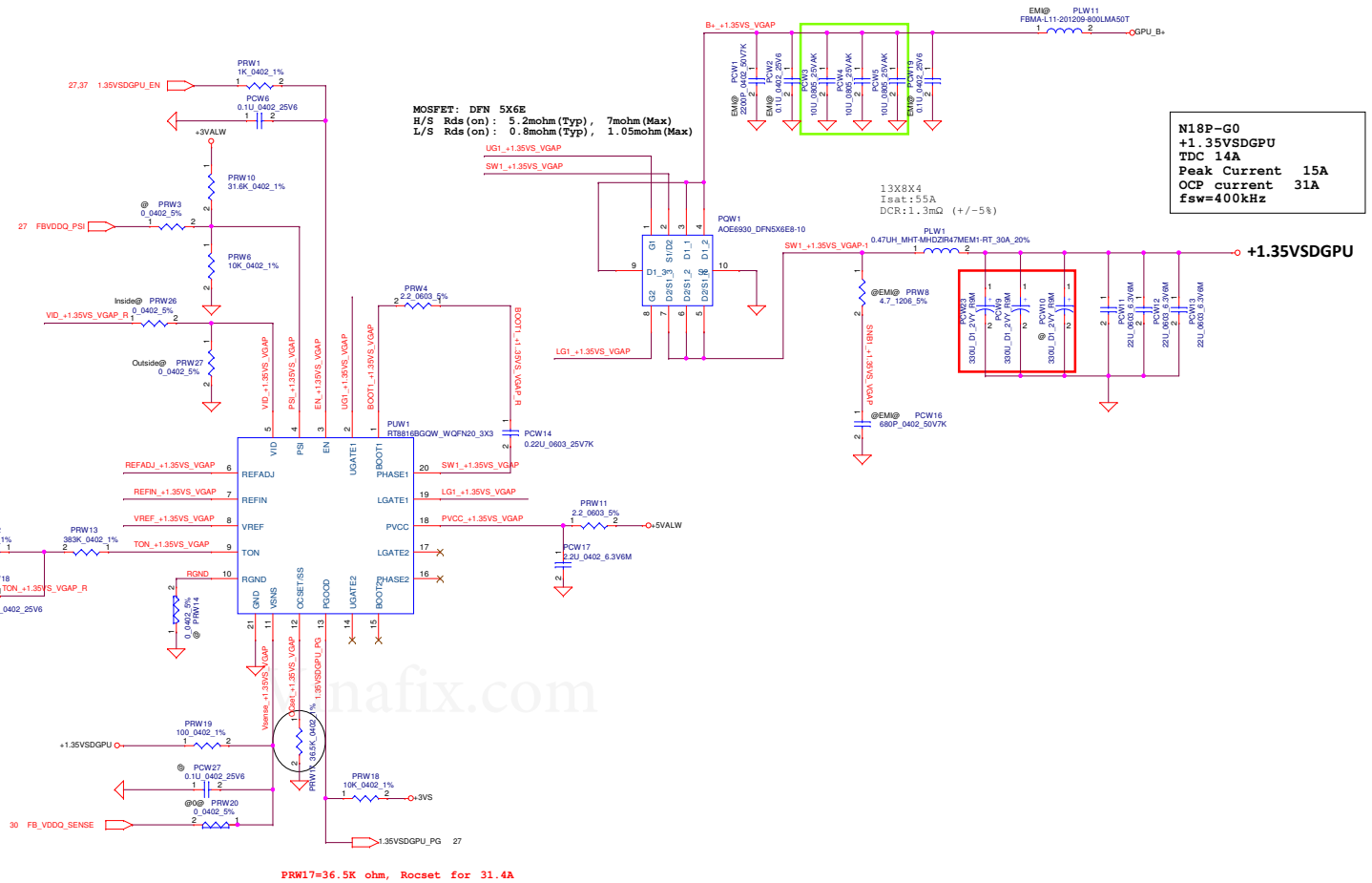
When, VRAM_VDD_CTL=Low
 $V_{boot} = 2 \cdot (30.9K // 68.1K) / (10K + (30.9K // 68.1K) + 80) = 1.356V \quad (x1.08)$



Micron & Hynix & Samesung VRAM

When, VRAM_VDD_CTL=High
 $V_{boot} = 1.515V \quad (x1.122)$

When, VRAM_VDD_CTL=Low
 $V_{boot} = 1.363V \quad (x1.091)$

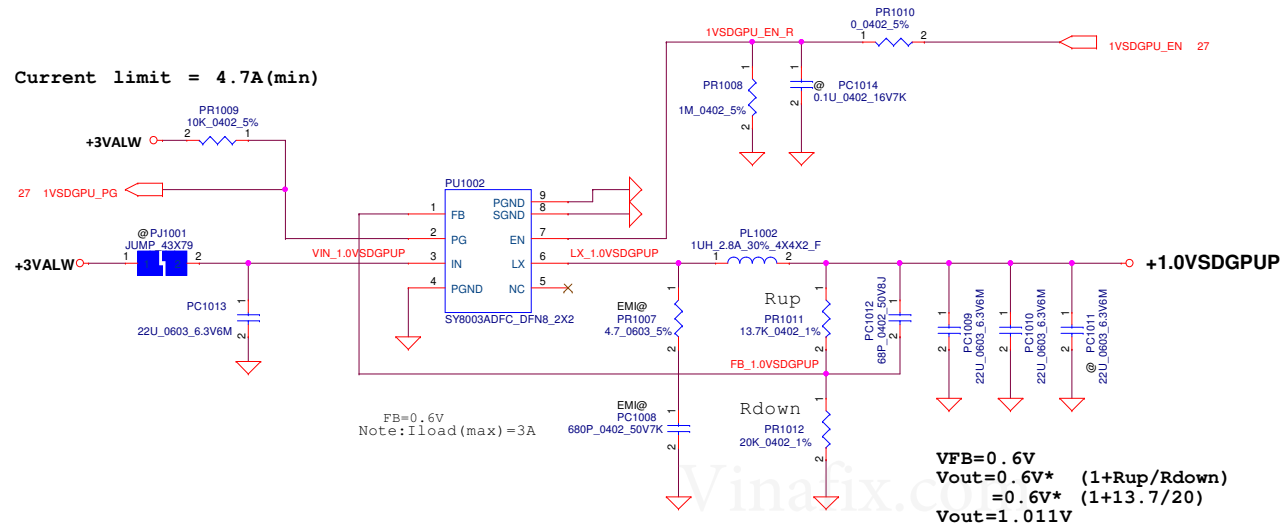


N18P-G0
+1.35VSDGPU
TDC 14A
Peak Current 15A
OCP current 31A
fsw=400kHz

PRW17=36.5K ohm, Rocset for 31.4A

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Current limit = 4.7A(min)



Choke 1uH SH00000YG00 (Common Part)
(Size:3.8 x 3.8 x 1.9 mm)
(DCR:20m~25m)

Choke: SH00000YG00 Size:4x4x2 (Common Part)
Rdc=27± 20% Taiyo
Rdc=20mohm(Typ), 25mohm(Max) Cyntec
Rdc=27± 20% 3L
Rdc=30± 20% Tai-Tech
Rdc=32± 20% Chilisin
Rdc=36mohm(Typ), Xmohm(Max) Maglayers

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)
=0.6V* (1+13.7/20)
Vout=1.011V

+1.0VSDGPUP → +1.0VSDGPU

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Version change
list (P.I.R. List)

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PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	Design Update	Solution Change	1.0	84	PQ301 change from 2N7002KW (SB000009Q80) to L2N7002SWT1G (SB00001GE00).	2019/09/18	C
02	Design Update	Solution Change	1.0	94	Add location PRW28, 10K_0402_1% (SD034100280)at net 'VRAM_VDD_CTL' and pull down.	2019/09/26	C
03	Design Update	Solution Change	1.0	84 86	PR312 change from 10_1206_5% (SD011100A80) to 10_0805_5% (SD002100A80). PC318 change from 100p_0603_50V (SE024101J80) to 100p_0402_50V (SE071101J80). PC301 change from 1000p_0603_50V (SE025102K80) to 1000p_0402_50V (SE074102K80). PC506,PC507 change from 10u_0603_6.3V (SE000005T80) to 10u_0402_6.3V (SE00000UD00).	2019/10/01	C
04	Design Update	Solution Change	1.0	82	PC101 change from 100p_0402_50V (SE071101J80) to 100p_0201_50V (SE00000SE00).	2019/10/01	C
05	Design Update	SDLE measure result	1.0	98	PR609 change from 24.3K_0402_1% (SD00000AT80) to 24.9K_0402_1% (SD034249280).	2019/10/07	C
	Design Update	SDLE measure result	1.0	90 88	Add location PC9101,PC9102,PC9103, 22U_0603_6.3V (SE00000M000)at net '+APU_CORE' and '+APU_CORE_SOC'. PR806 change from 52.3K_0402_1% (SD034523280) to 60.4K_0402_1% (SD034604280). PC807 change from 270p_0402_50V (SE074271K80) to 390p_0402_50V (SE074391K80). PC830 change from 330p_0402_50V (SE074331K80) to 390p_0402_50V (SE074391K80).	2019/10/14	C
06	Design Update	Solution Change	1.0	91 92 84	Change from 0 Ohm (0_0402_5%, SD028000080) to R-short as below location: PRV20,PRV34,PRV54,PRV56,PRV70,PRV145,PRV146,PRV79,PRV81,PRV84,PRV89,PRV91,PRV94,PRW9,PRW20, PR315,PR317,PR321,PR334, total 19 pcs.	2019/10/15	C
07	Design Update	Thermal team request	1.0	83	PR210 change from 16.9K_0402_1% (SD034169280) to 21K_0402_1% (SD034210280).	2019/10/15	PreMP
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
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Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
1	8		10/03	Change source	Change SA00004BV00 to SA0000BIO00 for UC64,UC65,UC66	PVT	1.0
2	9		10/03	Change source	Change SA000000H00 to SA0000BIP00 for UC4	PVT	1.0
3	27		10/03	Change source	Change SA00003R000 to SA0000BJI00 for UV2,UV10,UV11 Change RV9 from 100K_0402 to 10K_0402	PVT	1.0
4	37		10/03	Change source	Change SA00003R000 to SA0000BJI00 for UV46 Change SE082221J80 to SE074221K80 for CG335	PVT	1.0
5	42		10/03	Change source	Change SE082221J80 to SE074221K80 for CS129,CS130	PVT	1.0
6	52		10/03	Size reduce	Change CM79,CM80 from 10U_0603 to 10U_0402	PVT	1.0
7	56		10/03	Size reduce	Change SE071101J80 to SE00000SE00 for CA26 (0402 -> 0201)	PVT	1.0
8	58		10/03	Size reduce	Change SE071101J80 to SE00000SE00 for C1265,C1266,C1279 (0402 -> 0201)	PVT	1.0
9	68		10/03	Size reduce Change source	Change SE071101J80 to SE00000SE00 for CM17 (0402 -> 0201) Change SA000000H00 to SA0000BIP00 for UM5	PVT	1.0
10	78		10/03	Change source	Change SE082221J80 to SE074221K80 for CG336	PVT	1.0
11	68	PCIE SSD	10/04	SSD1_PCIE_RST# path change	Change UM5,RM135 to @ Change UM28 to pop	PVT	1.0
12	40	HDMI	10/14	Change footprint for colay 蓋綠漆	Change footprint,add"-npm" on R756,R765,L2513,L2514,L2515	PVT	1.0
13	66	IEC Thermal Sensor	10/23	THERMAL1_ALERT# need always PU	Change RF25 from TMSIEC@ to always pop	PVT	1.0

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2019/07/24		2020/07/24		HW PIR	
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